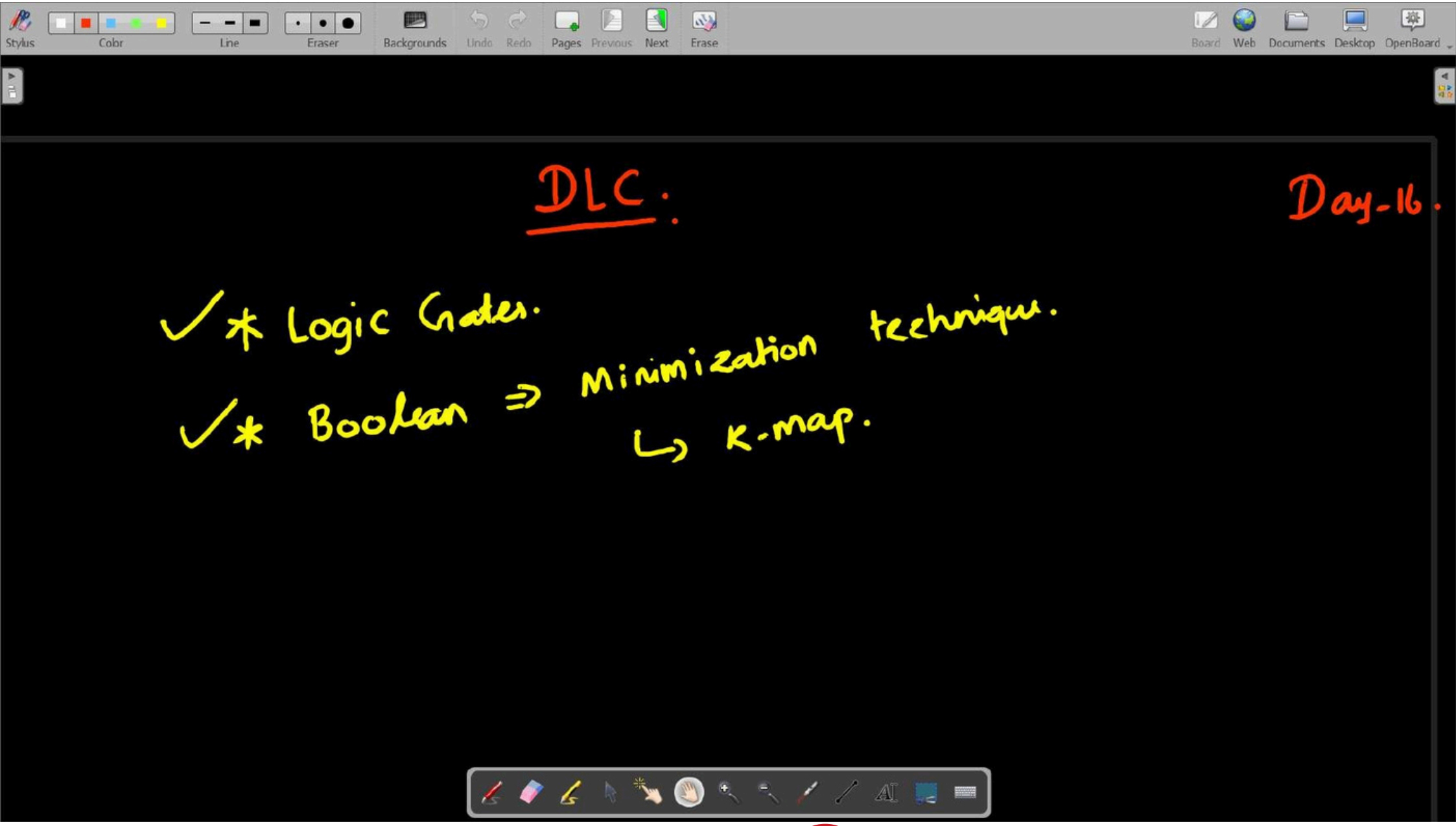

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Boolean expression (A + B)(A + C) is equal to

(a) AB + C (b) AC + B

(c) A + BC (d) ABC

UPPSC AE 2011, Paper-II

Q.2].

$Y = AA + AC + AB + BC$.

$= A + AC + AB + BC$.

(c)

$= A[1 + C] + AB + BC$

$= A + AB + BC$

$= A[1 + B] + BC$.

$= A + BC$

$AA = A$.

$A = 1$

$1 \times 1 = 1$

$A = 0$.

$0 \times 0 = 0$.

$1 + A = 1$

$1 + 1 = 1$

$1 + 0 = 1$

0.5 x

Full Video Link

The simplified form of the Boolean function Y
$= \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + AB\overline{C}$

(a) $\overline{C}$ (b) C

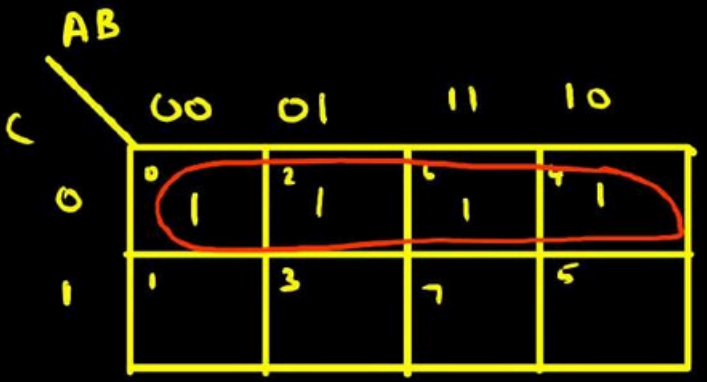
(c) $\overline{AB}$ (d) AB

TNPSC AE 2018

Q.3]. $Y = \Sigma m(0, 2, 4, 6)$.

$= \overline{C}$ (A).

000 + 010 + 100 + 110.



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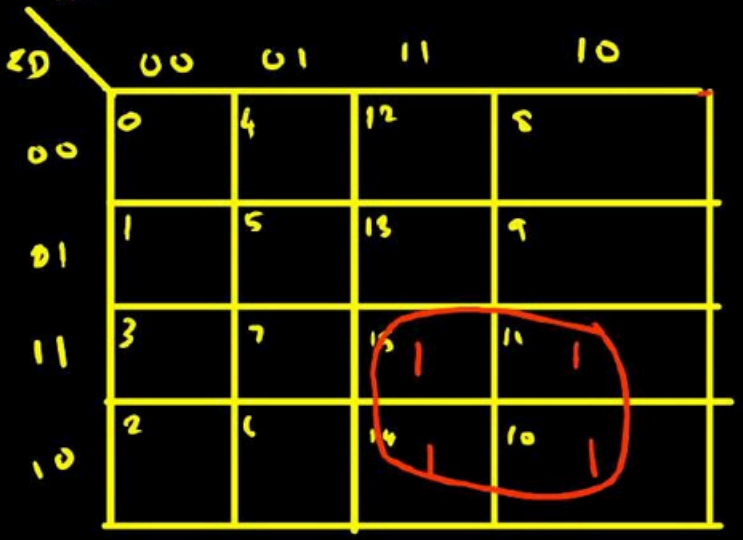
II.

$Y = 1111, 1011, 1110, 1010.$

$Y = \Sigma m(10, 14, 11, 15).$



$Y = CA = AC$

The Boolean expression $ABCD + A\bar{B}CD + ABC\bar{D} + A\bar{B}C\bar{D}$ is equivalent to-

(a) A (b) AC

(c) ABC (d) 1

RPSC AE 2018

(b).

I $Y = ABCD + A\bar{B}CD + ABC\bar{D} + A\bar{B}C\bar{D}$

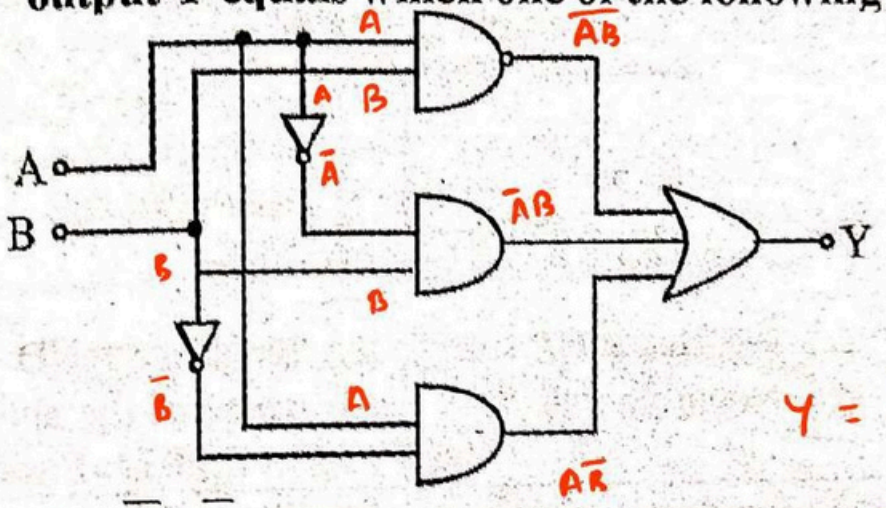
$= ACD[B+\bar{B}] + AC\bar{D}[B+\bar{B}].$

$= ACD + AC\bar{D} = Ac[D+\bar{D}].$

$= AC.$

Full Video Link

In the circuit shown in the figure below, the output Y equals which one of the following?



(a) $\bar{A}+\bar{B}$
(b) $A+B$
(c) $\bar{A}B+A\bar{B}$
(d) AB

BPSC Poly. Lect. 2016
ESE 2008

NAND = $\overline{AB}$

(A)

$Y = \bar{A}B + \bar{A}B + A\bar{B}$.

$= \bar{A} + \bar{B} + \bar{A}B + \bar{B}A$.

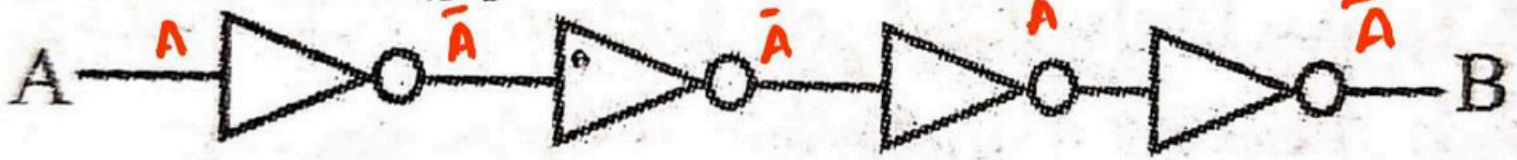
$= \bar{A}[1+B] + \bar{B} + \bar{B}A$.

$= \bar{A} + \bar{B}[1+A]$.

$= \bar{A} + \bar{B}$.

Full Video Link

The output at point B if the input at point A is a 0 bit will be



(a) neither 1 nor 0
(b) either 1 or 0
(c) 0
(d) 1

$\bar{\bar{A}}$

B = A

B = 0

Rajasthan Nagar Nigam AE 2016 Shift-III

(c)

Full Video Link

The output of a logic gate is 1 when all its inputs are at logic 1. The gate is either

(a) an OR or an EX-OR
(b) an OR or an EX-NOR
(c) a NAND or an EX-NOR
(d) an AND or a NAND

UPPSC AE 2008, Paper-I

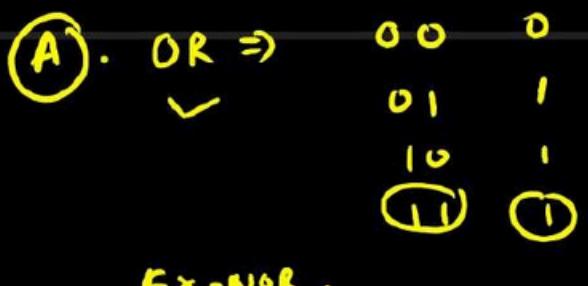
(b)

$= A \oplus B = A\bar{B} + \bar{A}B$

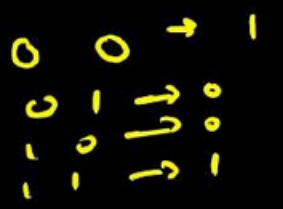
01 + 10

10 + 10

(A) OR ⇒



(B) EX-NOR.



$= A \odot B = AB + \bar{A}\bar{B}$

$= 0 \times 0 + 1 \times 1 = 1$

$= 1 \times 1 + 0 \times 0 = 1 + 0 = 1$

Full Video Link

Which of the following is equivalent to the Boolean expression (XYZ+YZ+XZ)?

(a) X (b) Y

(c) Z (d) (X+Y)Z

UPRVUNL AE 2016

Q.8]. $A = xyz + yz + xz$. (d).

$= yz[x+1] + xz$.

$= yz + xz$.

$= z[x+y]$.

II :

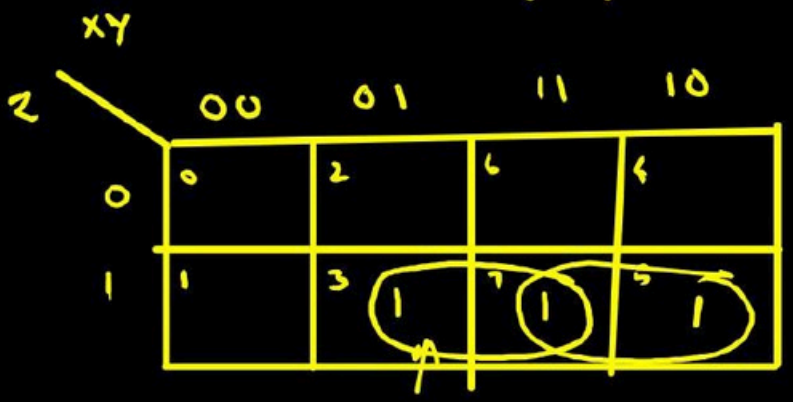
$A = xyz + yz[x+\bar{x}] + xz[y+\bar{y}]$.

$= xyz + xyz + \bar{x}yz + xy\bar{z} + x\bar{y}z$.

$= xyz + \bar{x}yz + x\bar{y}z$.

$= 111 + 011 + 101$.

$A = \Sigma m(7, 3, 5)$.

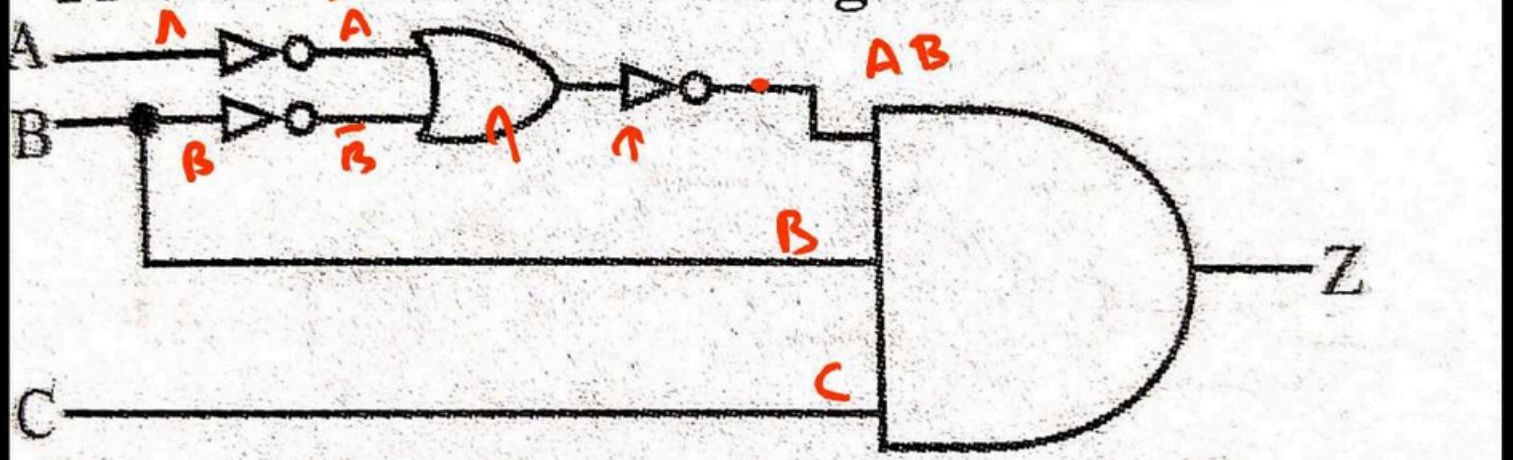


$A = zx + zy$.

$= xz + yz$.

Full Video Link

Find the value of Z in the given circuit.



(a) ABC
(b) (A') (B) C
(c) 0
(d) (A') BC

UPRVUNL AE 2016

$\bar{A}$, $\bar{B}$ => A, B — $(\overline{A+B})$

$\overline{(\bar{A}+\bar{B})}$

$= \bar{\bar{A}} \cdot \bar{\bar{B}} = AB$.

$Z = AB.B.C$

$= ABC$.

Q.9. (A).

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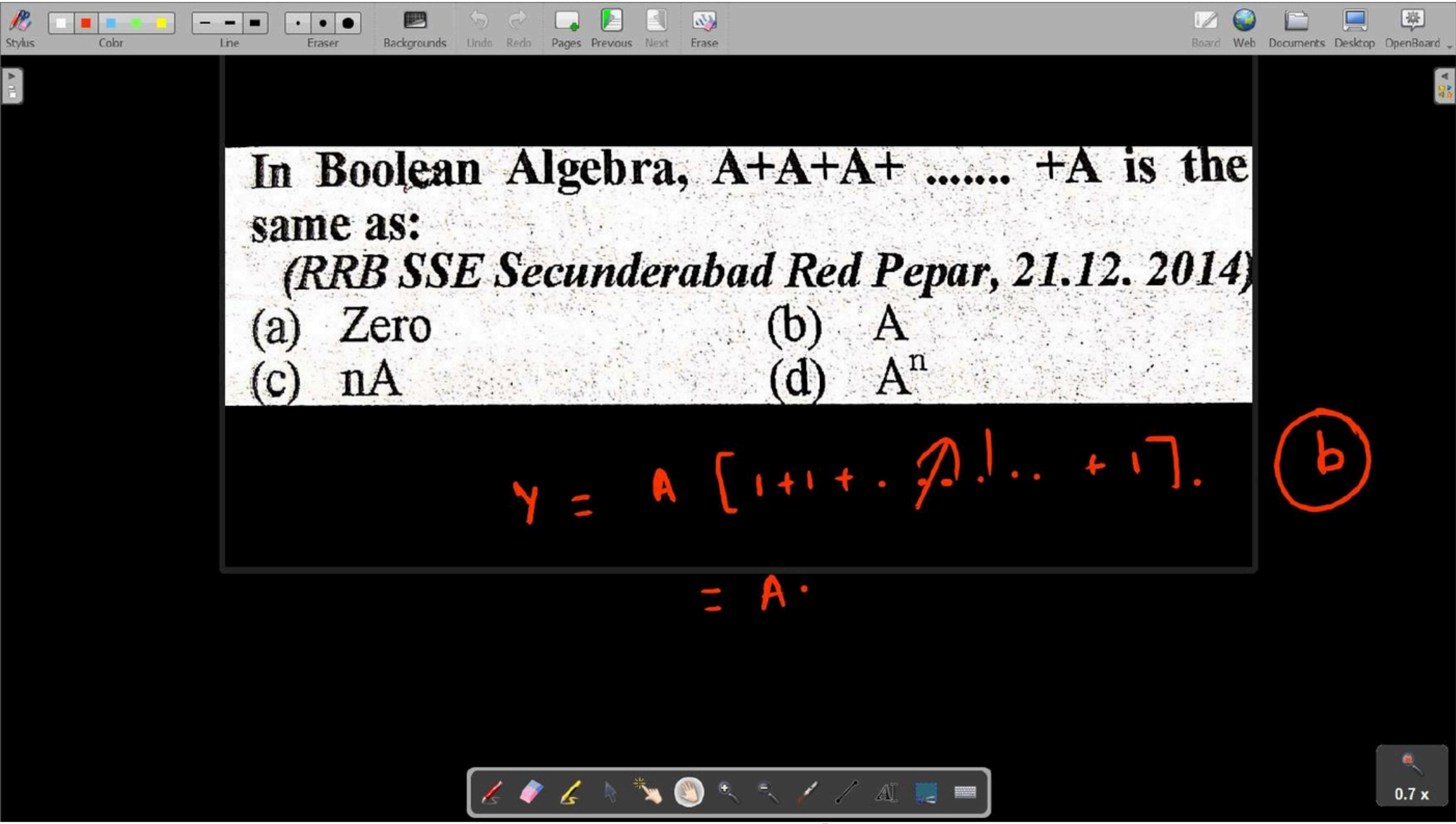

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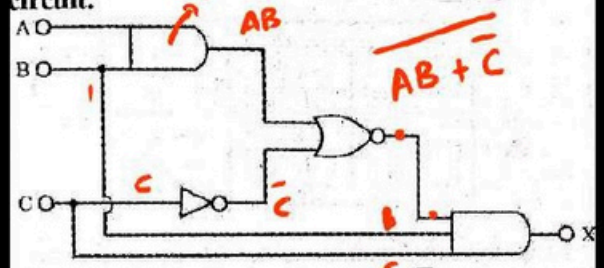
Find the output Boolean function for the logic circuit.



(a) X= ABC
(b) X= $\bar{A}BC$
(c) X= $\bar{A}\bar{B}C$
(d) X= $\bar{A}BC$

UPPCL AE 04-11-2019 Shift I

Q.1]. (B)

$X = \overline{(AB + \bar{C})}(B)(C)$.

$= (\bar{A}\bar{B} \cdot \bar{\bar{C}})(B)(C)$. $A \cdot A \cdot A \cdot A = A$.

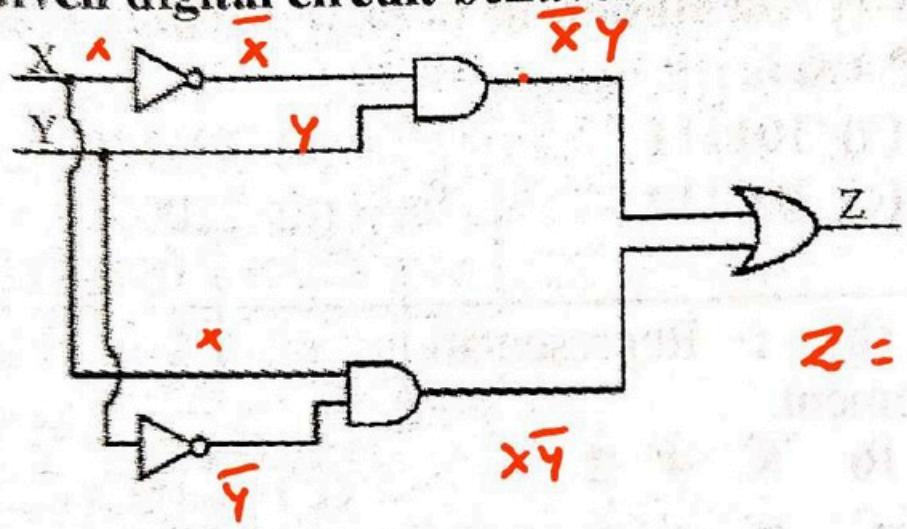
$= (\bar{A} + \bar{B})CB$

$= \bar{A}BC + \bar{B}BC = \bar{A}BC$.

0.4 x

Full Video Link

Given digital circuit behaves as an:



(a) OR gate
(b) XOR gate
(c) NOR gate
(d) NAND gate

UPPCL AE 04-11-2019 Shift I

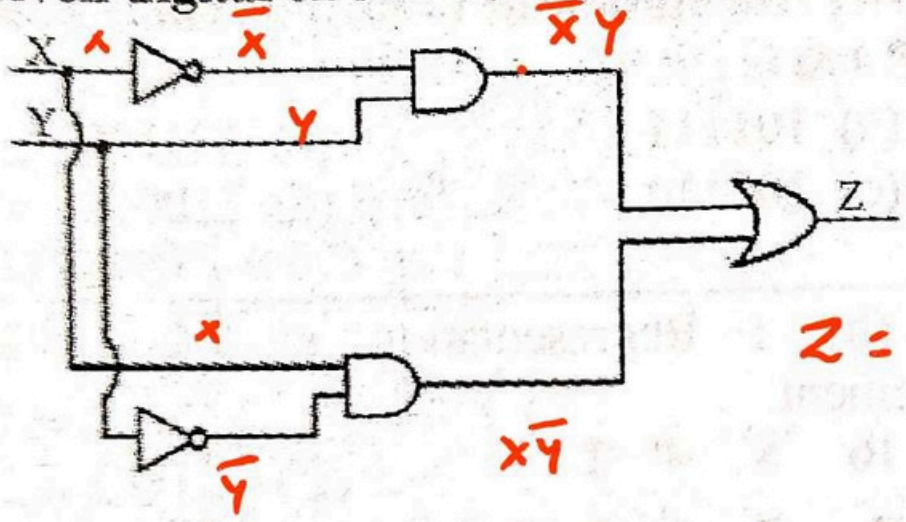
B.

$Z = \bar{X}Y + X\bar{Y}$.

$= X \oplus Y$ = EXOR.

Full Video Link

Given digital circuit behaves as an:



(a) OR gate
(b) XOR gate
(c) NOR gate
(d) NAND gate

UPPCL AE 04-11-2019 Shift I

B.

$Z = \bar{X}Y + X\bar{Y}$.

$= X \oplus Y$ = EXOR.

Full Video Link

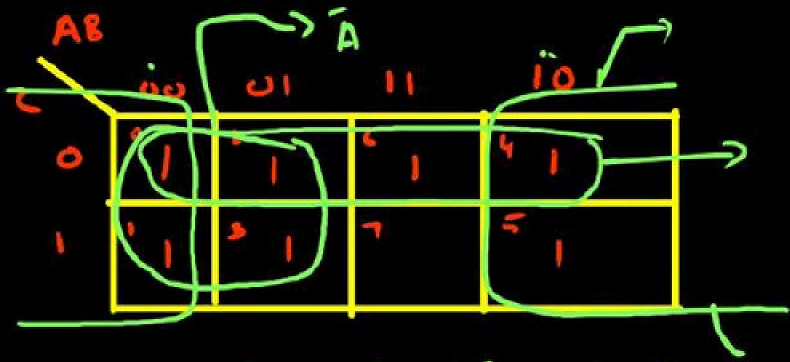
A combination circuit is described by a function as the sum of min-terms. The function is defined as $f(A,B,C) = \Sigma m(0,1,2,3,4,5,6)$

A is the MSB and C is the LSB. The minimized expression of the function is.

(a) ABC (b) $\overline{B}+\overline{C}$

(c) $\overline{A}+\overline{B}+C$ (d) $\overline{A}+\overline{B}+\overline{C}$

UPPCL AE 01-01-2019 Shift I

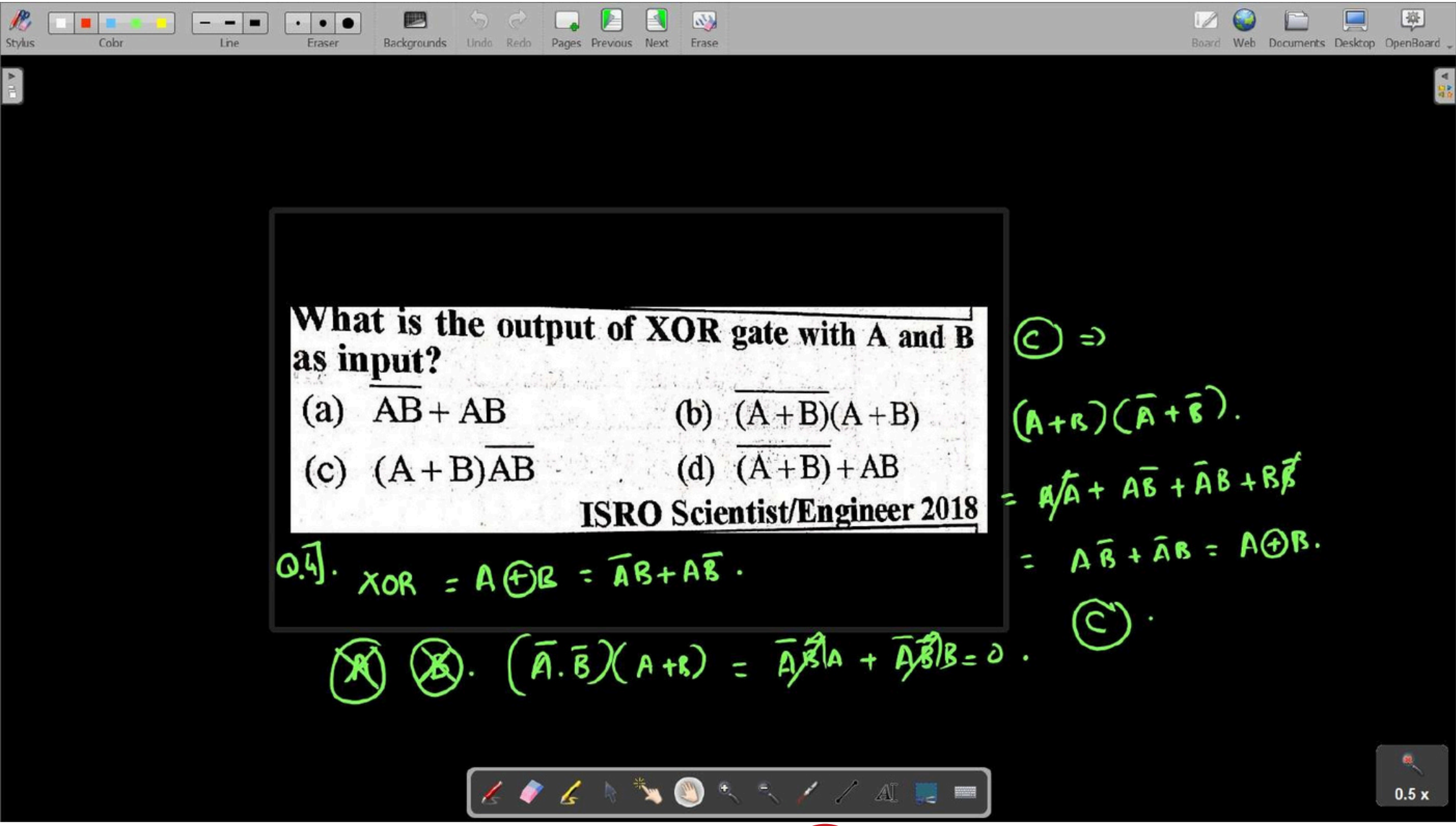


$f(A,B,C) = \overline{A} + \overline{C} + \overline{B}.$

$= \overline{A}+\overline{B}+\overline{C}.$

Q.3]. $f(A,B,C) = \Sigma_m (0,1,2,3,4,5,6).$

(d).



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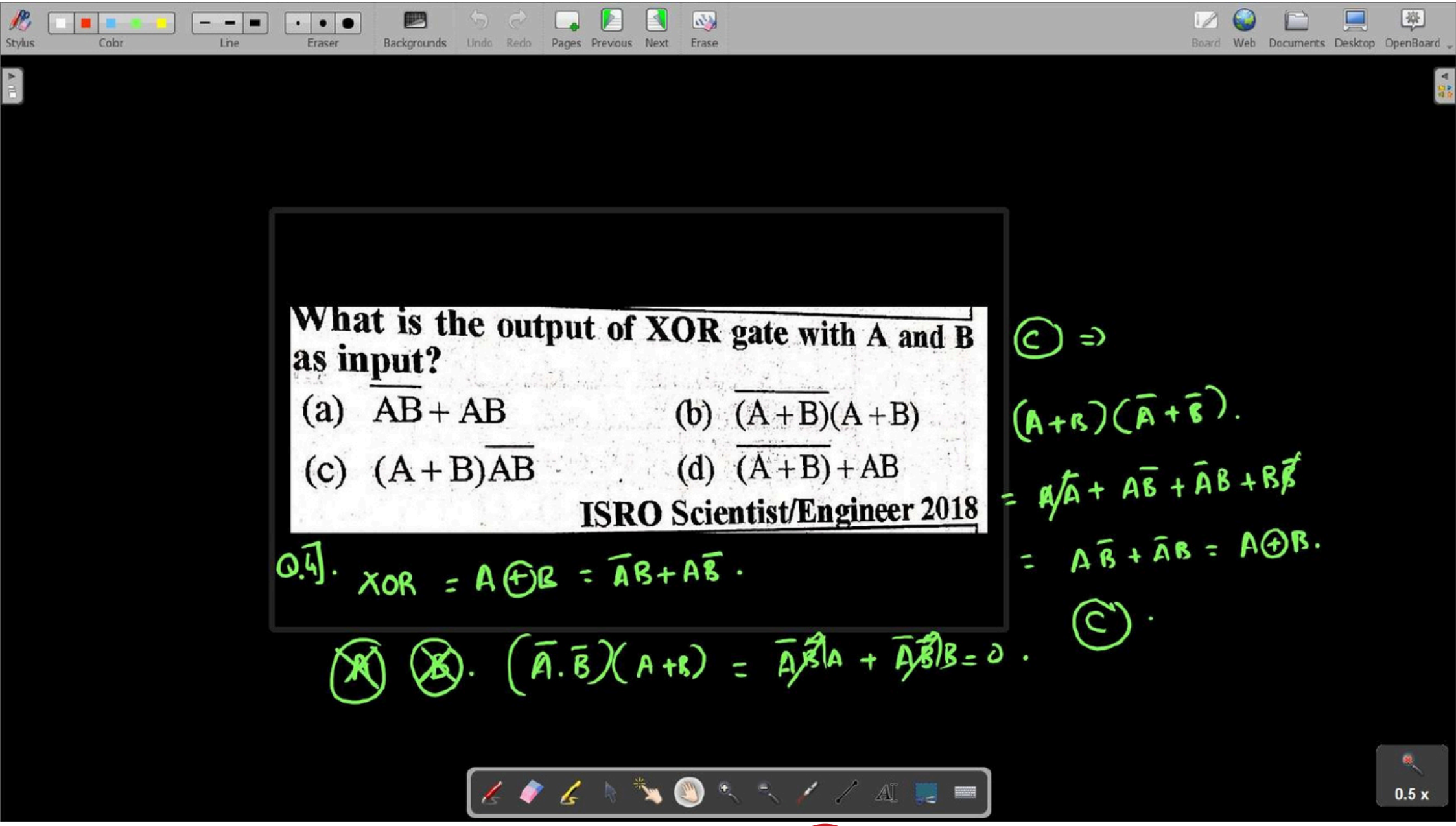
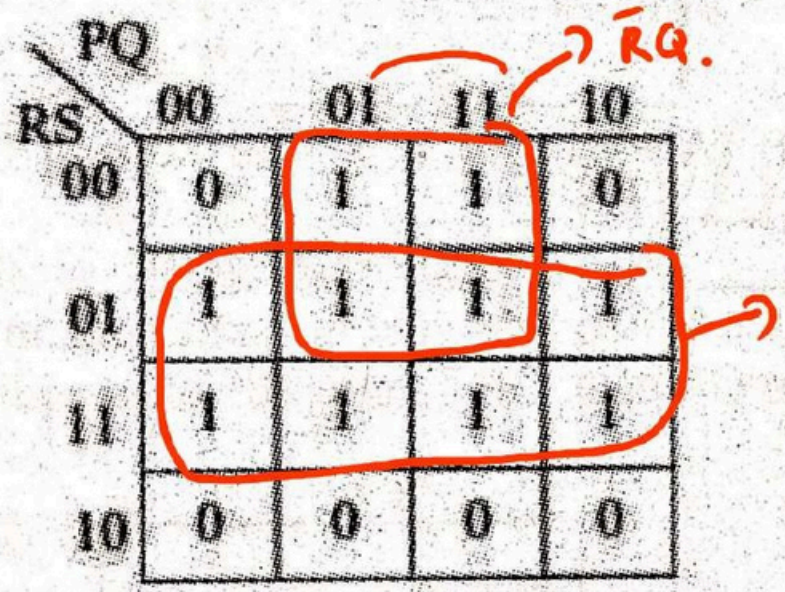


Full Video Link

Q5].

Find suitable option for the given k-map



(a) $Q\bar{R}+S$

(b) $QR+S$

(c) $Q\bar{R}+\bar{S}$

(d) $QR+\bar{S}$

UPPCL AE 04-11-2019 Shift I

$= Q\bar{R} + S.$

A.

$2^4 = 16.$

$2^3 = 8.$

$2^2 = 4$

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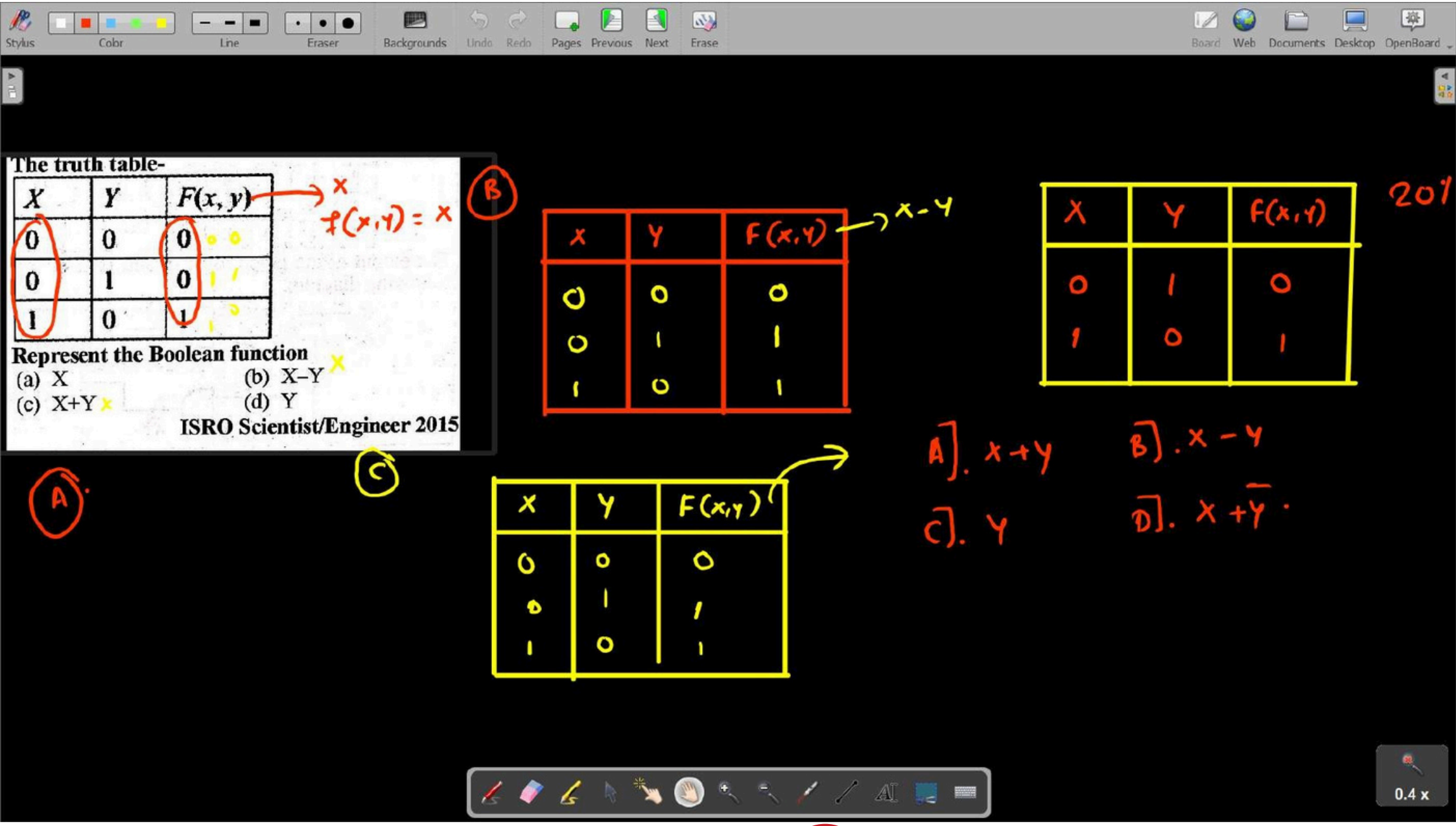

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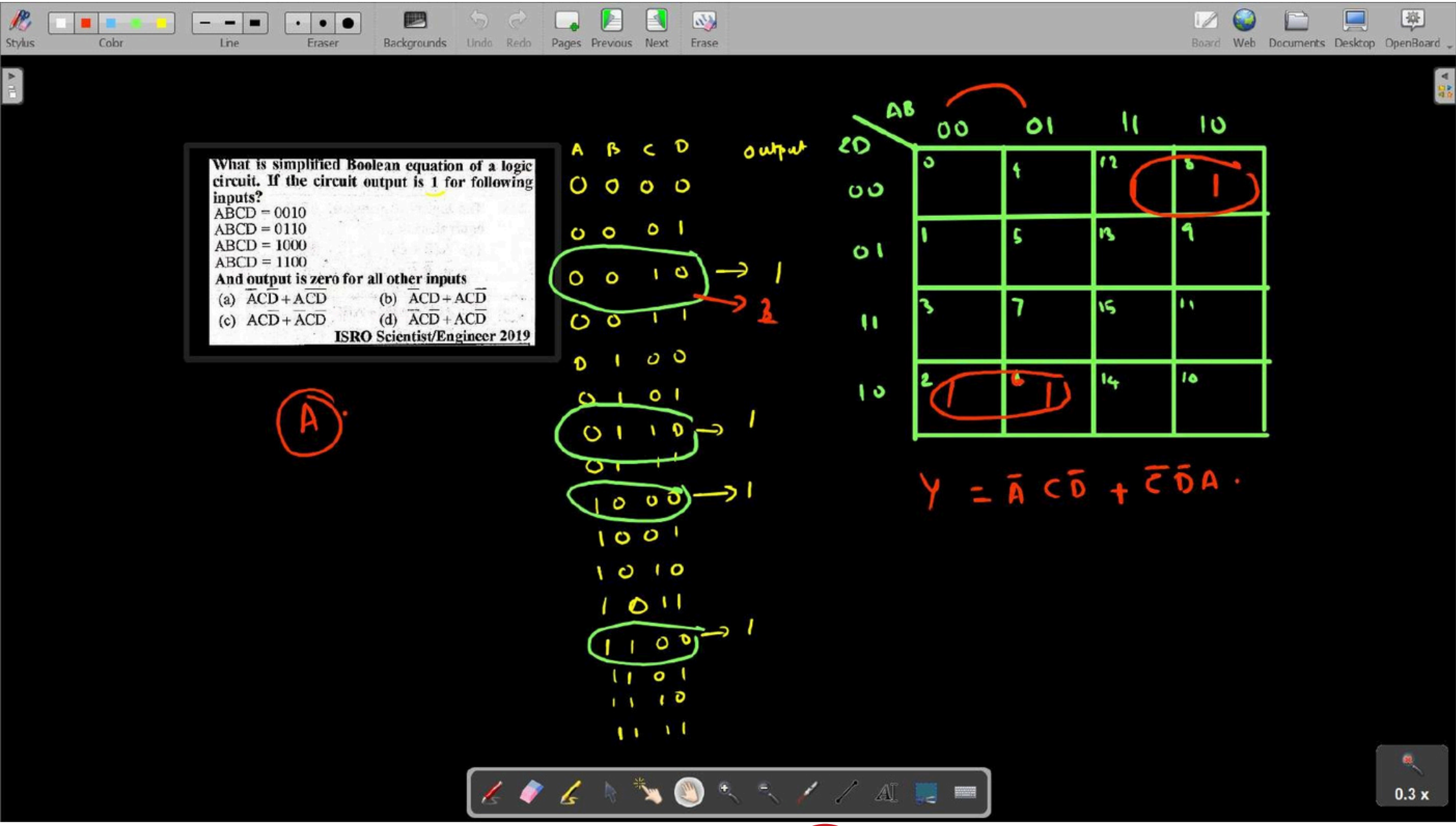

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$f(A,B,C) = ABC$

A B f

$f(A,B) =$

The Truth table for the function f(ABCD) = $\Sigma m(0, 1, 3, 4, 8, 9)$ is

A	B	C	f
0	0	0	W
0	0	1	X
0	1	0	Y
0	1	1	0
1	0	0	Z
1	0	1	0
1	1	0	0
1	1	1	0

Where W, X, Y, Z are given by (d is the complement of D)

(a) D, d, 1, 1 (b) 1, d, D, 1

(c) 1, 1, D, d (d) 1, D, d, 1

ESE 2018

$f(ABCD) = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D.$

$f(ABC) = \bar{A}\bar{B}\bar{C}W + \bar{A}\bar{B}CX + \bar{A}B\bar{C}Y + A\bar{B}\bar{C}Z.$

$f(ABCD) = \bar{A}\bar{B}\bar{C}[D+\bar{D}] + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}[D+\bar{D}].$

$= \bar{A}\bar{B}\bar{C}1 + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}$

$W = 1$ $\quad Y = \bar{D} = d$

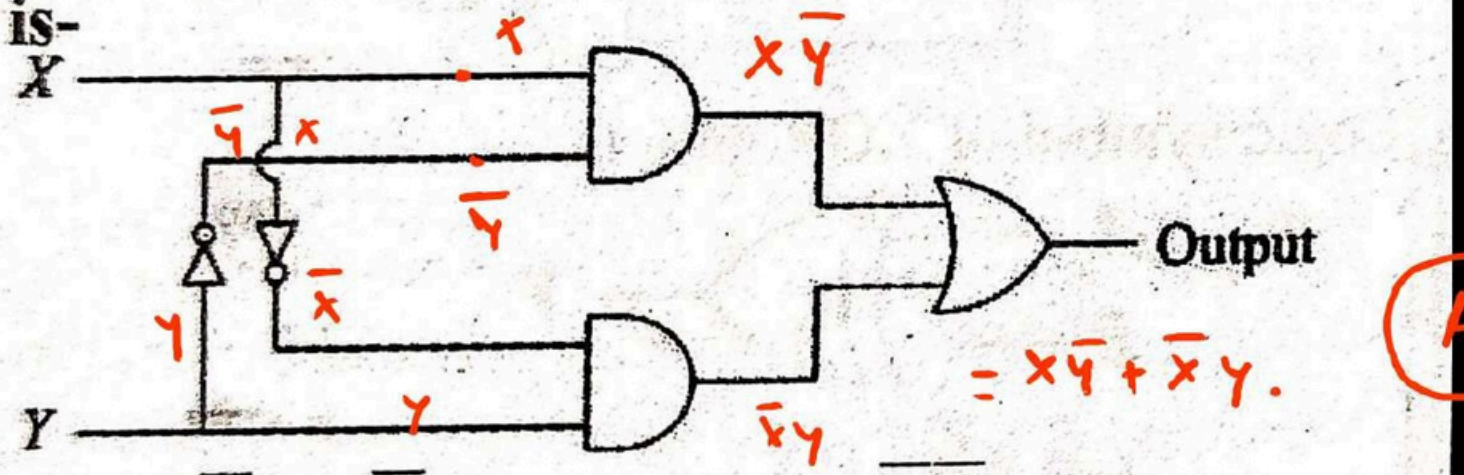
$X = D.$ $\quad Z = 1$

1, D, d, 1

0.4 x

Full Video Link

The logic evaluated by the circuit at the output is-



$= x\bar{y} + \bar{x}y$.

A

(a) $X\bar{Y} + Y\bar{X}$

(b) $\overline{X\bar{Y}} + XY$

(c) $\overline{(X+Y)}XY$

(d) $\overline{X}Y + X\overline{Y} + X + Y$

ISRO Scientist/Engineer 2015

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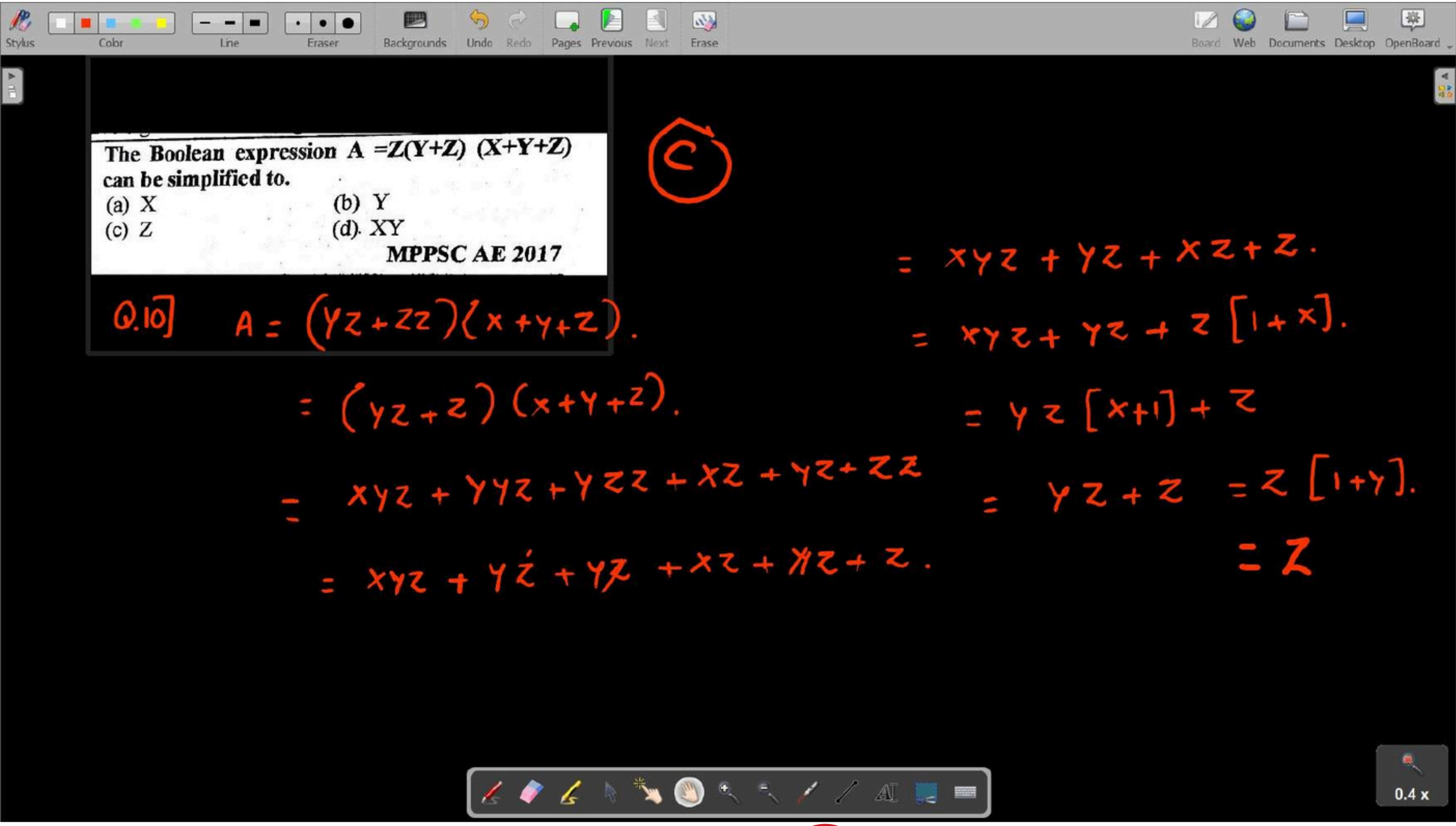

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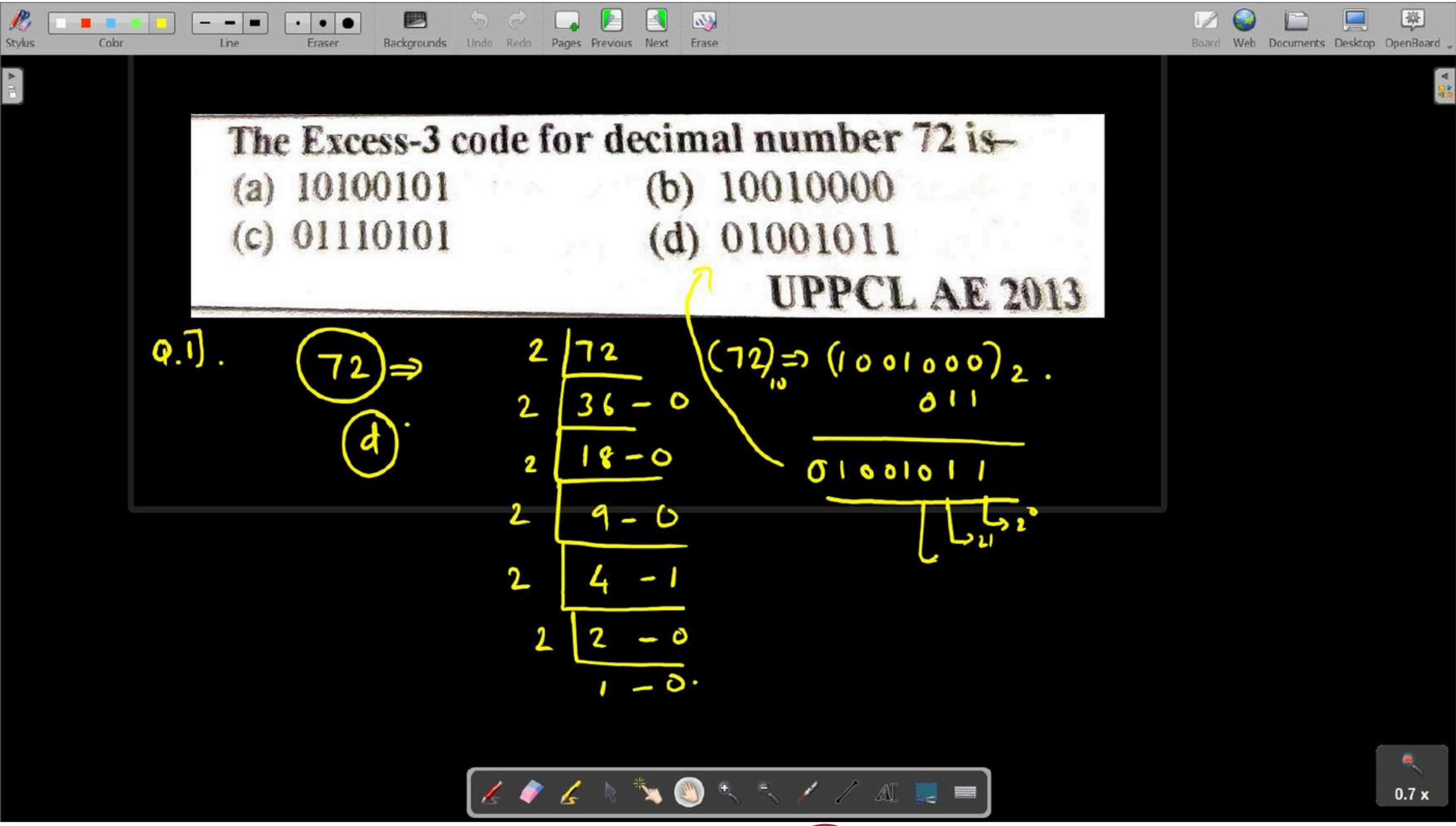

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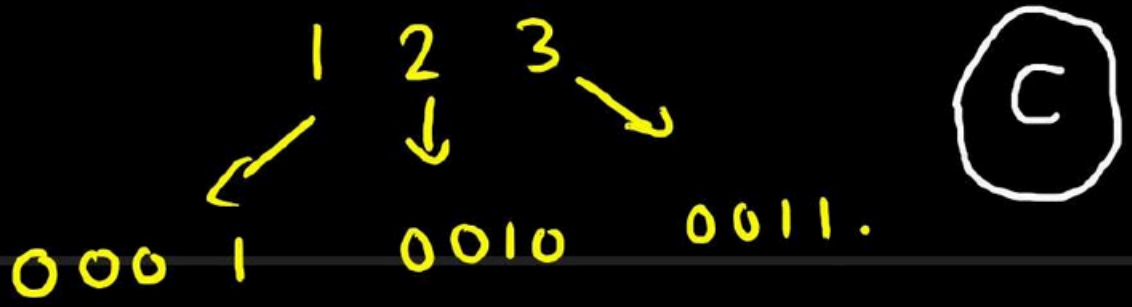
The BCD of 123 is:

(a) 000100110010 (b) 001010011

(c) 000100100011 (d) 011011

UPSC Poly. Lect. 2019

Q.2].



C

C.

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Which among the following is the decimal equivalent of hex number 1A53?

(a) 6793 (b) 6739

(c) 6973 (d) 6379

UPRVUNL AE 2014

hexa => 1 A 5 3.
10

0001 1010 0101 0011

$1\times2^0 \rightarrow 1$

$1\times2^1 \rightarrow 2$

$1\times2^4 \rightarrow 16$

$1\times2^6 \rightarrow 64$

$1\times2^9 \rightarrow 512$

$1\times2^{11} \rightarrow 2048$

$1\times2^{12} \rightarrow 4096$

b

$2^6\times2^2 = 64\times4$

$= 256$

$2^6\times2^3 = 64\times8$

$512\times$

$2^{11} = 2^9\times2^2$

$= 512\times4$

$2^{12} = 2^{11}\times2$

$= 2048\times2$

Full Video Link

Which among the following is the decimal equivalent of hex number 1A53?

(a) 6793 (b) 6739

(c) 6973 (d) UPRVUNL AE 2014

hexa => 1 A 5 3

0001 1010 0101 0011

$1\times2^0 \rightarrow 1$

$1\times2^1 \rightarrow 2$

$1\times2^4 \rightarrow 16$

$1\times2^6 \rightarrow 64$

$1\times2^9 \rightarrow 512$

$1\times2^{11} \rightarrow 2048$

$1\times2^{12} \rightarrow 4096$

6739

b

$2^6\times2^2 = 64\times4$

$=256$

$2^6\times2^3 = 64\times8$

$=512\times4$

$2^{11} = 2^9\times2^2$

$=512\times4$

$2^{12} = 2^{11}\times2$

$=2048\times2$.

$2^{12} =>$

2

Full Video Link

How many 1's are present in the binary representation of $(256\times7)+(4\times16)+(9\times4096)+5$

(a) 8 (b) 11

(c) 9 (d) 10

UPPCL AE 2013

A · Q.4

$(16^2\times7)+(4\times16)+(9\times16^3)+5\times16^0$.

$9\times16^3+7\times16^2+(4\times16)+5\times16^0$

$(9\ 7\ 4\ 5)_{16}$

16
16 | 3
96
16
256 | 3
16
150 6
25 6
1 9

How many 1's are present in the binary representation of $(256\times7)+(4\times16)+(9\times4096)+5$

(a) 8 (b) 11

(c) 9 (d) 10

UPPCL AE 2013

A · Q.4

$(16^2\times7)+(4\times16)+(9\times16^3)+5\times16^0$

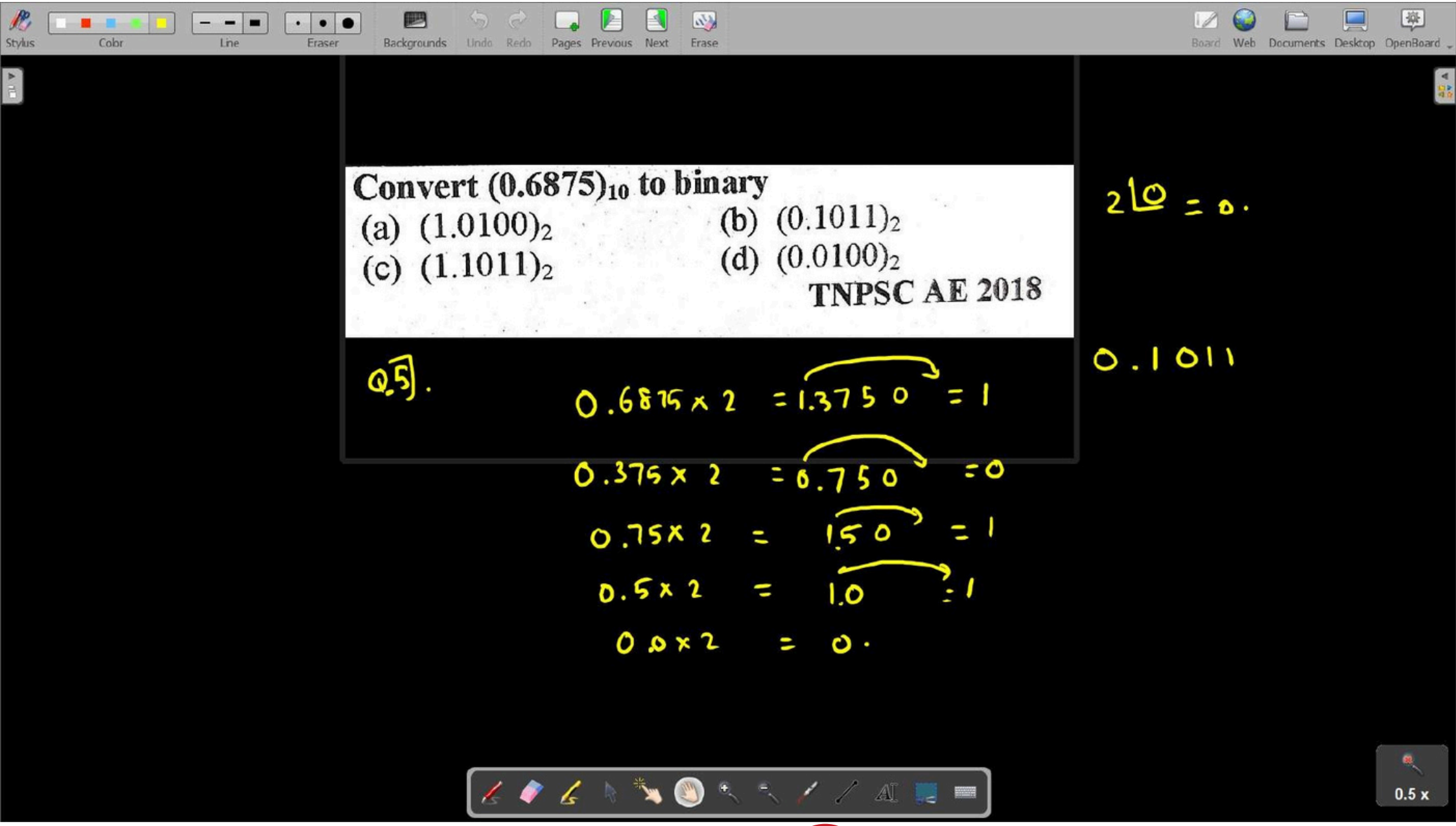
$9\times16^3+7\times16^2+(4\times16)+5\times16^0$

$(9\ 7\ 4\ 5)_{16}$

1001 0111 0100 0101

9 7 4 5

16 | 16 | 3 | 96 | 1 | 6 | 256 | 3 | 16 | 150 | 6 | 25 | 6 | 1 | 6



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$(734)_8 = (?)_{16}$

(a) C1D
(b) DC1
(c) 1CD
(d) 1DC

UPRVUNL AE 2014

10 - A
11 - B
12 → C
13 → D

Q.6]. $(734)_8$ → Hexa.

$(734)_8 = (111011100)_2$

$(111\ 011\ 100)_2 \Rightarrow 13$

1 13 12.

1 D C.

Full Video Link

Using 10's complement, subtract : (52532-3250)

(a) 49282 (b) 149282

(c) 85578 (d) 161828

TNPSC AE 2018

0.7.

52532

3250

49282

A

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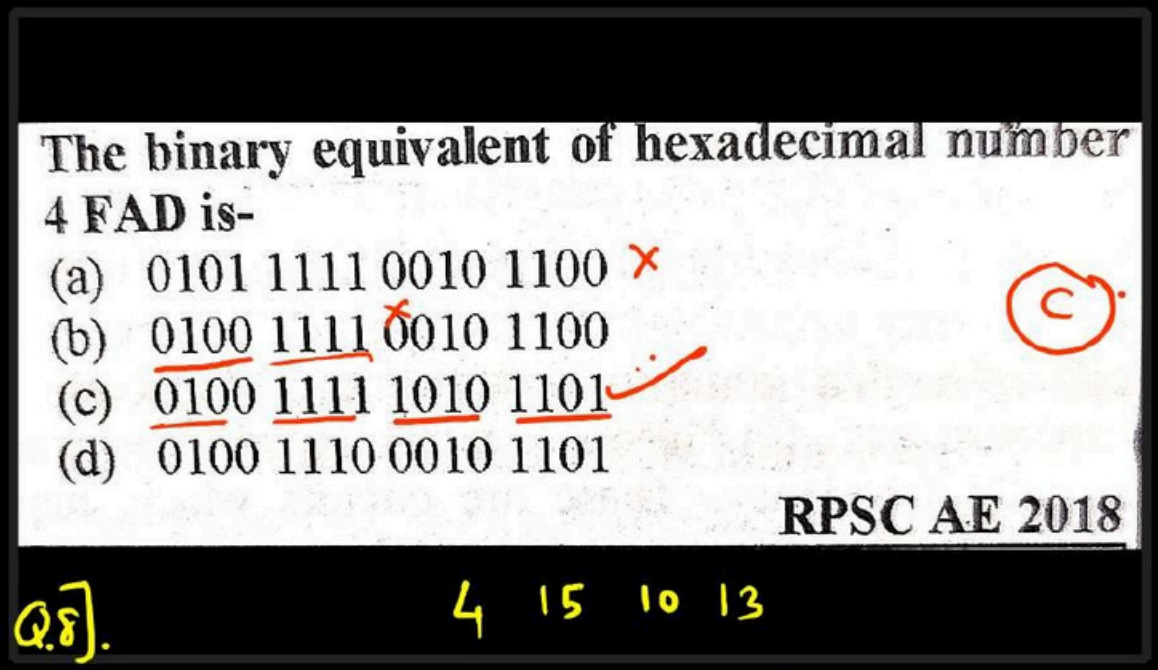

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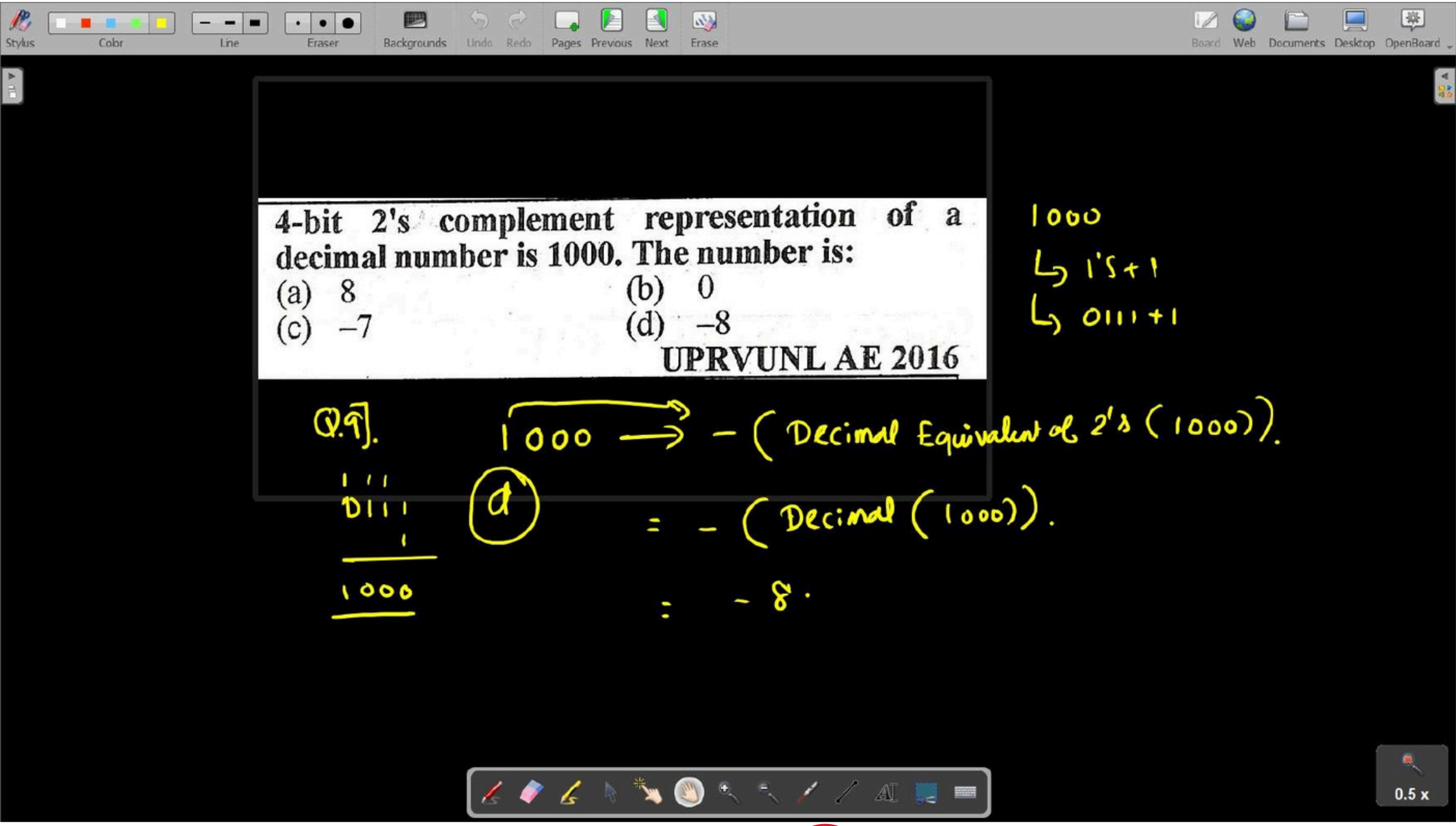


Full Video Link

The binary representation of the decimal number 1.375 is :

(a) 1.111 (b) 1010

(c) 1.011 (d) 1.001

UPRVUNL AE 2016

Q.10]. 1.375 . $2(1 \rightarrow (1.011)_2$. (c) .

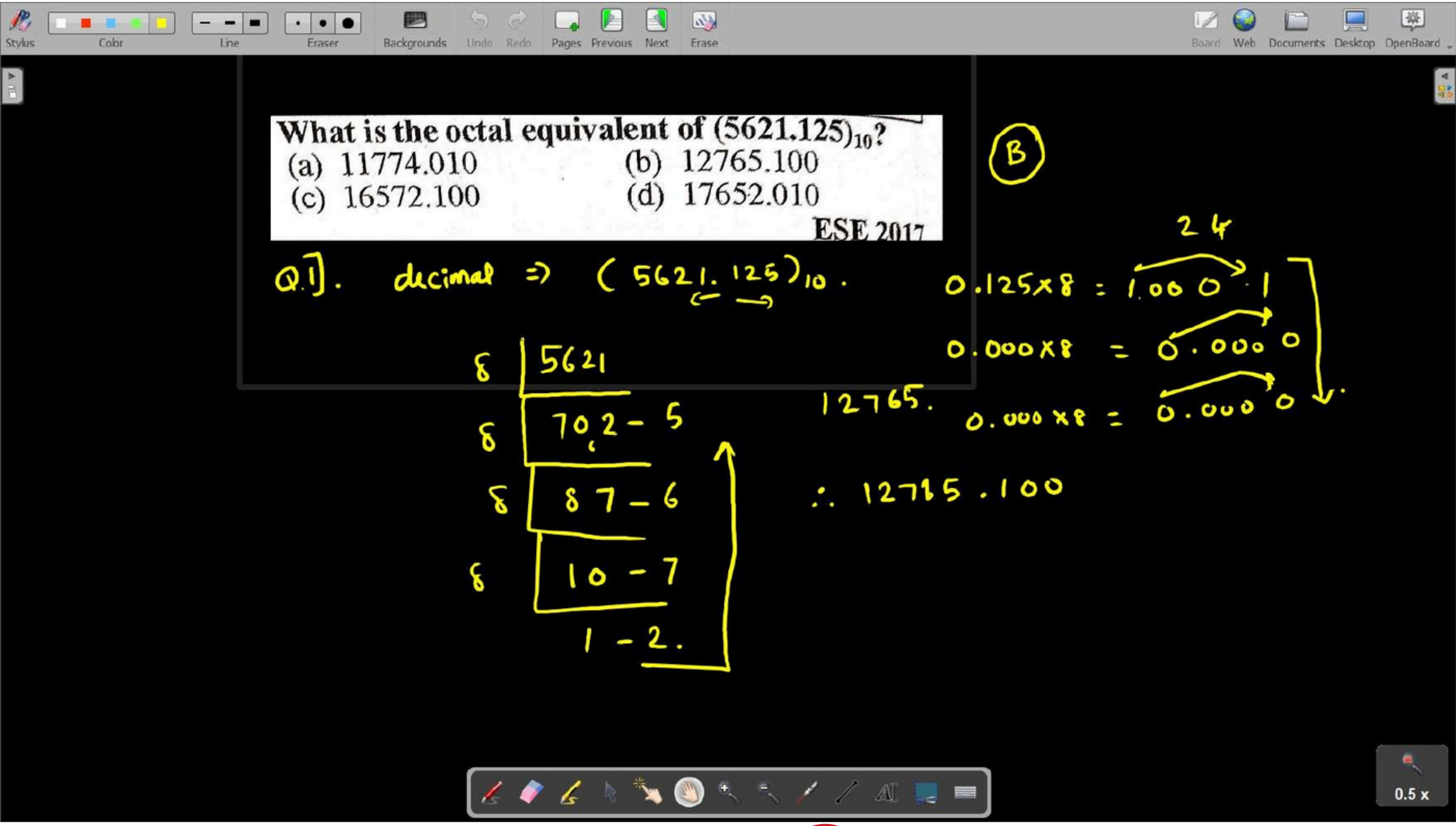
$0.375 \times 2 = 0.750 = 0$

$0.750 \times 2 = 1.500 = 1$

$0.5 \times 2 = 1.0 = 1$

$0.0 \times 2 = 0.$

Full Video Link



Full Video Link

The decimal equivalent of binary number 1001.101 is

(a) 9.750 (b) 9.625

(c) 10.750 (d) 10.625

ESE 2019

Q.2]. (b)

$(1001.101) \rightarrow$

$1 \times 2^0 = 1$

$1 \times 2^3 = 8$

9

(9.625)

0.101

1×2^{-1}

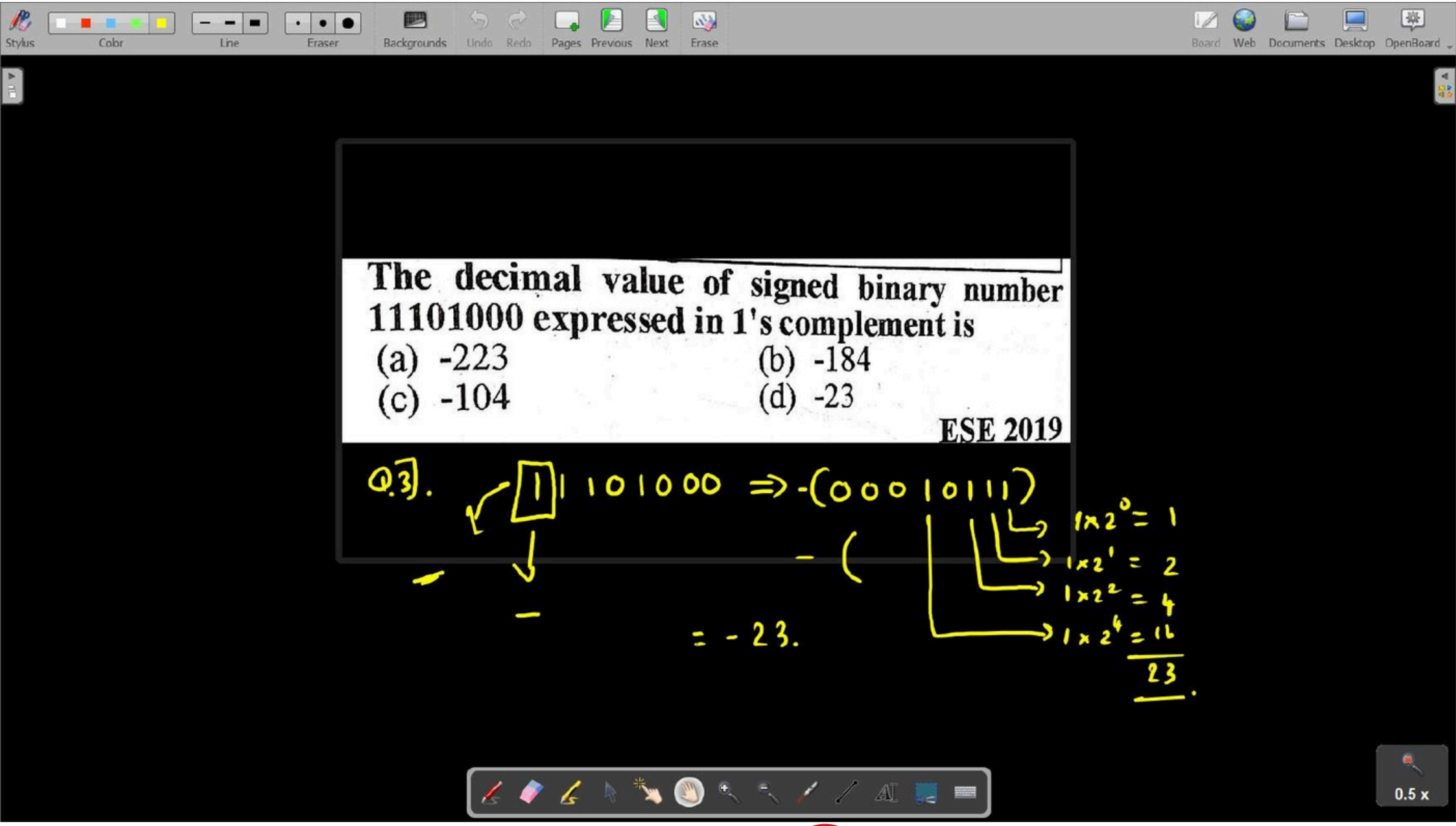
1×2^{-3}

$\frac{1}{2} + \frac{1}{2^3} = \frac{1}{2} + \frac{1}{8} = \frac{4+1}{8}$

$= \frac{5}{8}$

0.625

Full Video Link


The decimal value of signed binary number 11101000 expressed in 1's complement is
(a) -223
(b) -184
(c) -104
(d) -23
ESE 2019
Q.3.
1 101000 ⇒ -(00010111)
= -23.
1×2^0 = 1
1×2^1 = 2
1×2^2 = 4
1×2^4 = 16
23.
Full Video Link

What is the hexadecimal representation of $(657)_8$?

(a) 1 AF
(b) D 78
(c) D 71
(d) 32 F

ESE 2017

(A).

Q.4]. $(657)_8 \Rightarrow$

$(110\ 101\ 111)_2$

0001 1010 1111

(10) (15)

1 A F.

Full Video Link

Convert decimal 41.6875 into equivalent binary:

(a) 100101.1011 (b) 100101.1101

(c) 101001.1011 (d) 101001.1101

ESE 2019

Q.5] 41.6875.

(C)

2	41
2	20 - 1
2	10 - 0
2	5 - 0
2	2 - 1
	1 - 0

$0.6875 \times 2 = 1.3750 = 1$

$0.375 \times 2 = 0.750 = 0.$

$0.75 \times 2 = 1.50 = 1$

$0.5 \times 2 = 1.0 = 1.$

101001.1011

Full Video Link

What is the octal equivalent of hexadecimal number CD.AB?

(a) 320.506 (b) 215.546

(c) 205.516 (d) 315.526

ISRO Scientist/Engineer 2018

Q.6. $(CD.AB)_{16}$

$(1100\ 1101.\ 1010\ 1011)_2$

1100 1101. 1010 1011

(d)

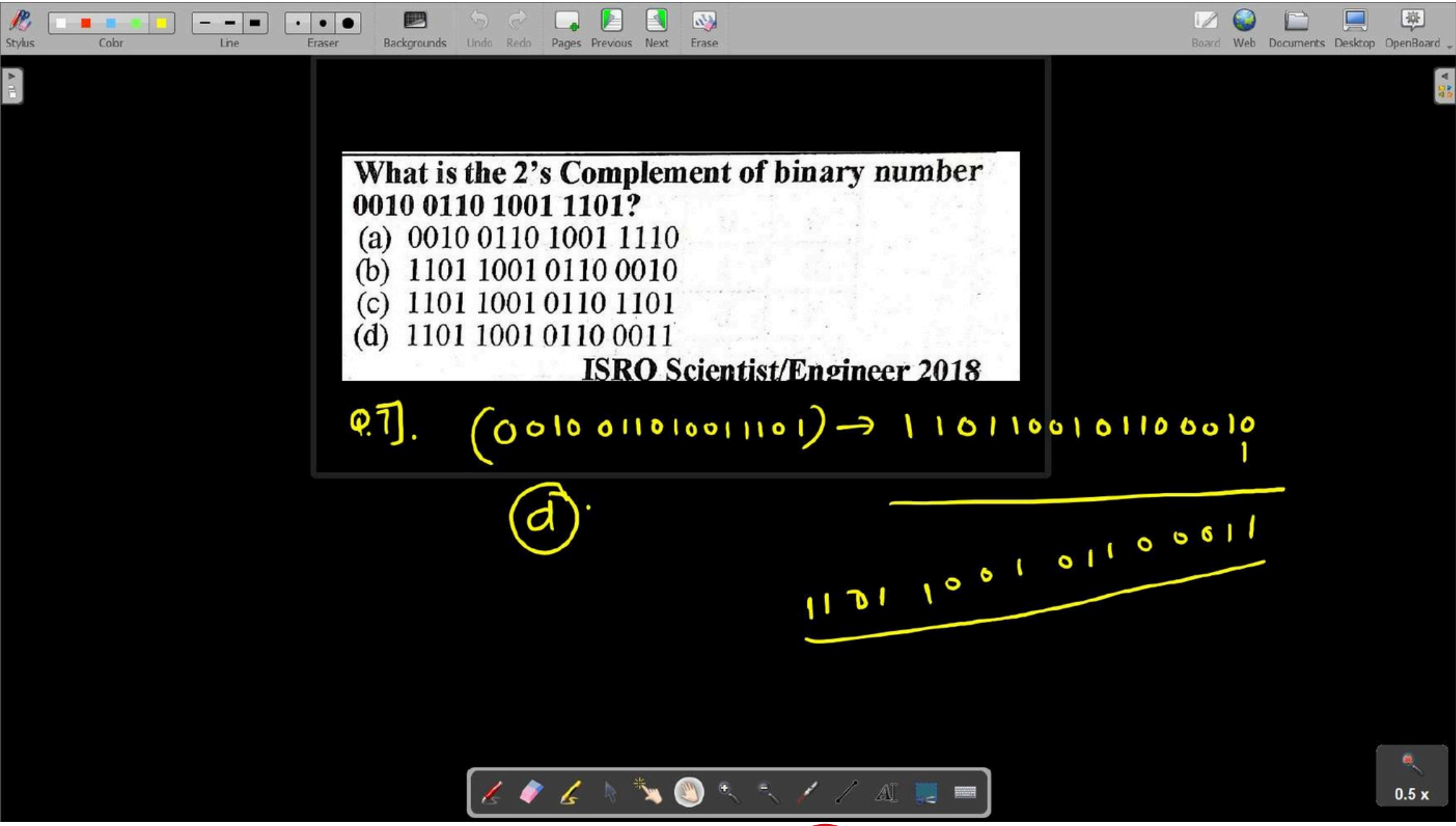
1 2 3 4 5 6 7 8 9 A

B C D E F.

110

315. 526.

Full Video Link



Full Video Link

Representation of $(-20)_{10}$ in two's complement form is :

(a) 101111 (b) 101100

(c) 101110 (d) 110001

BHEL ET 2019

Q.8]. $(-20)_{10}$ $\rightarrow$ $(10100) \Rightarrow 01011$ $+1$ $= 01100$.

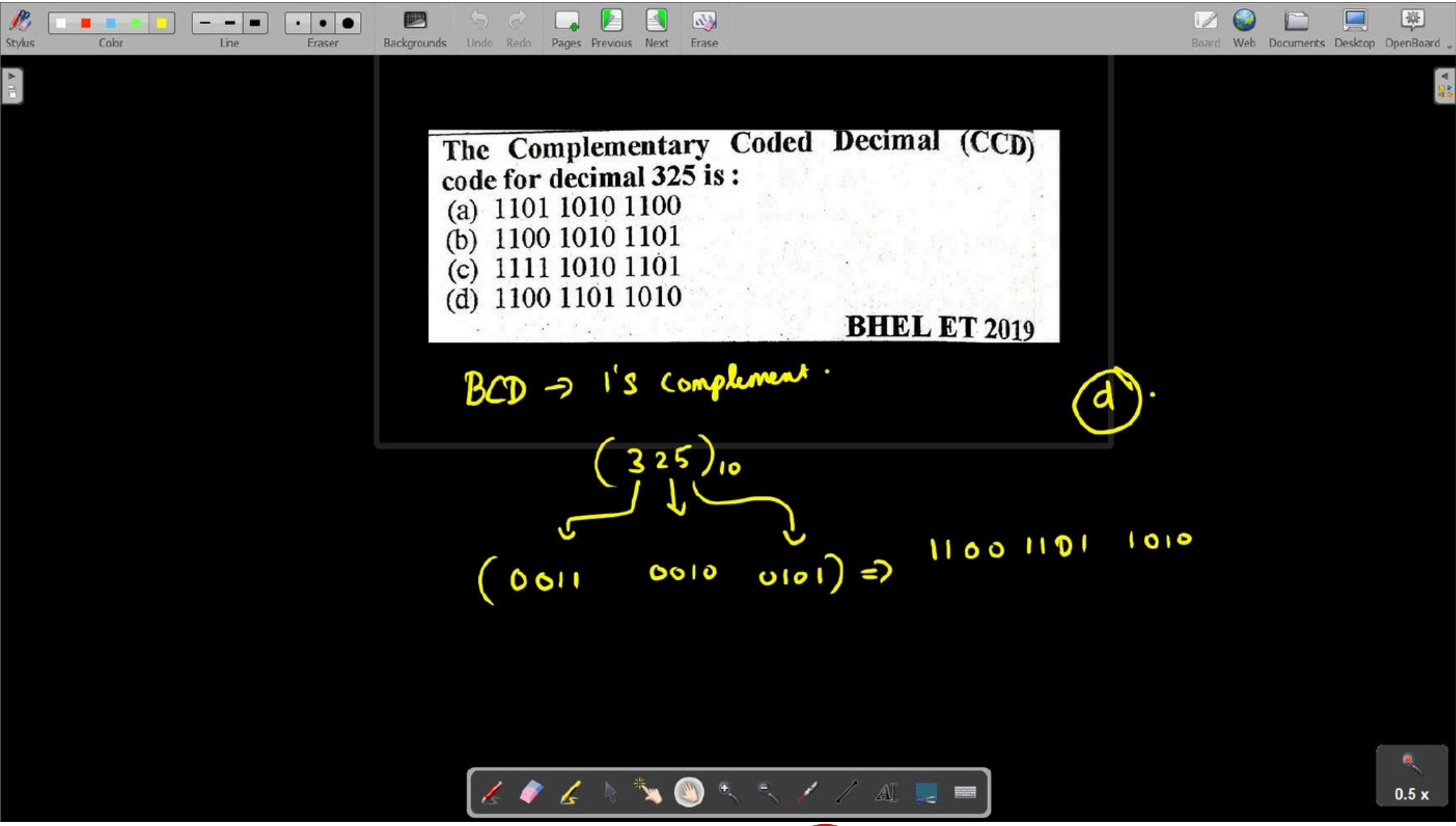
$01100 \rightarrow 10$ 1100

(b)

$(-17)_{10}$. $\rightarrow$ 1

$(17)_{10} \Rightarrow (10001) \rightarrow 01110$ $+1$ $= 01111$

Full Video Link



Full Video Link

The equivalent decimal number of $(0.4051)_8$ is :

(a) 0.5100098 (b) 0.6100018

(c) 0.4100028 (d) 0.70108

BHEL ET 2019

Q.10]. $(0.4051)_8 \Rightarrow 0.$

4×8^{-1}

5×8^{-3}

1×8^{-4}

$= \frac{4}{8} + \frac{5}{512} + \frac{1}{4096}$

$= \frac{2048 + 40 + 1}{4096} = \frac{2089}{4096}.$

$= 0.51000097$

(A)

Combinational Circuit.

Adders.

1. Half Adders:

Sum = $A \oplus B$ Carry = AB.

2. Full Adder:

Sum = $A \oplus B \oplus C_{in}$ Carry = $AB + C[A \oplus B]$.

Here C is not a input [carry].

3. Full Adder Using Half Adder:

2 Half Adders + one OR gate require.

Full Video Link

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Combinational Circuit.

Adders.

1. Half Adder:

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Here C is not a input [carry].

3. Full Adder using Half Adder:

2 Half Adders + one OR gate require.

4. Half Subtractor:

Difference = $A \oplus B$ Borrow = $\bar{A}B$.

5. Full subtractor:

Difference = $A \oplus B \oplus C$ Borrow = $\bar{A}[B+C] + BC$

1.4 x

Full Video Link

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4. Half Subtracton:

Difference = $A \oplus B$ Borrow = $\bar{A}B$.

5. Full subtracton:

Difference = $A \oplus B \oplus C$ Borrow = $\bar{A}[B+C] + BC$

Half Addus → NAND Gate → 5
Half Substracton NOR gate → 5

Full Addus → NAND gate → 9
Full Substractor NOR gate → 9.

6. Carry Look Ahead Addu:

$C_0 = AB + C(A \oplus B)$.

2.0 x

Full Video Link

A full substractor can be constructed from two half substractors and a –

(a) 2-input NAND gate (b) 2-input NOR gate

(c) 2-input OR gate (d) 2-input AND gate

UKPSC AE 2012 Paper-II

Q.1 (c)

0 0 0

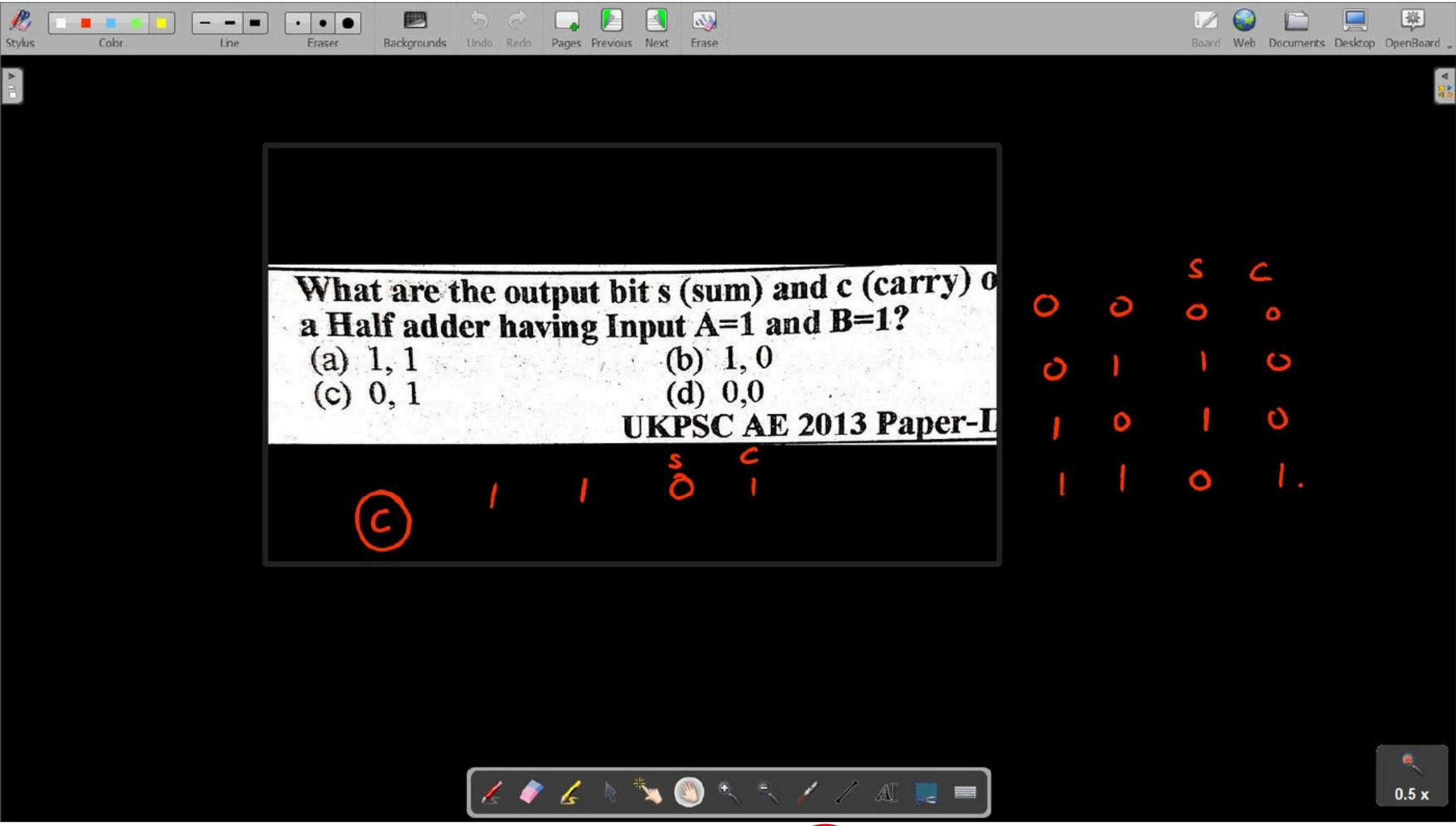
0 0 1

A

B

C

Full Video Link



Full Video Link

An 8:1 multiplexer has how many select inputs?

(a) 2 (b) 1

(c) 3 (d) 8

UPPCL AE 01-01-2019 Shift II

16 x 1 → 2^4

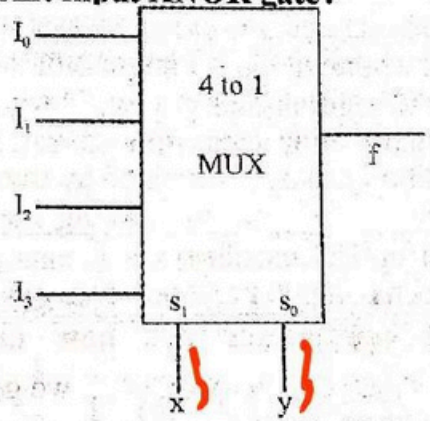
32 x 1 → 2^5

Q.3. (c)

$8 = 2^n \Rightarrow n = 3$

Full Video Link

Which logic inputs should be given to the input lines I_0, I_1, I_2 and I_3, if the MUX is to behave as two point input XNOR gate?



(a) 0110
(b) 1001
(c) 1000
(d) 1111

ESE 2017

$XNOR = \bar{x}\bar{y} + xy$

$XOR = x\bar{y} + \bar{x}y$.

$f = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$.

$f = \bar{x}\bar{y} I_0 + \bar{x}y I_1 + x\bar{y} I_2 + xy I_3$.

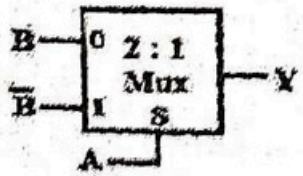
(b).

1 0 0 1
I_0 I_1 I_2 I_3

$f = \bar{x}\bar{y} + xy$

Full Video Link

The following 2:1 multiplexer block implements?



(a) An AND gate
(b) An Ex-NOR gate
(c) An OR gate
(d) An Ex-OR gate

Rajasthan Nagar Nigam AE 2016 Shift-III

Q.5]. $Y = \bar{S}B + S\bar{B}$

$= \bar{A}B + A\bar{B}$.

$= A \oplus B$.

(d)

Full Video Link

The half adder circuit has the following number of inputs and outputs respectively.

(a) 1,2
(b) 2,1
(c) 2,2
(d) 2,3

MPPSC AE 2017

Q.1.

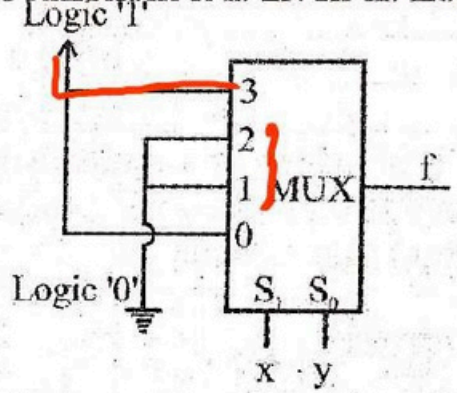
2 → Inputs.

2 → outputs.

(c).

Full Video Link

The output f of the 4-to-1 MUX is shown in the figure. The function. f. is given as Logic '1'



(a) $\bar{x}\bar{y} + xy$ (b) $\bar{x}y + x\bar{y}$

(c) $x+y$ (d) $\bar{x}+\bar{y}$

UPPCL AE 01-01-2019 Shift II

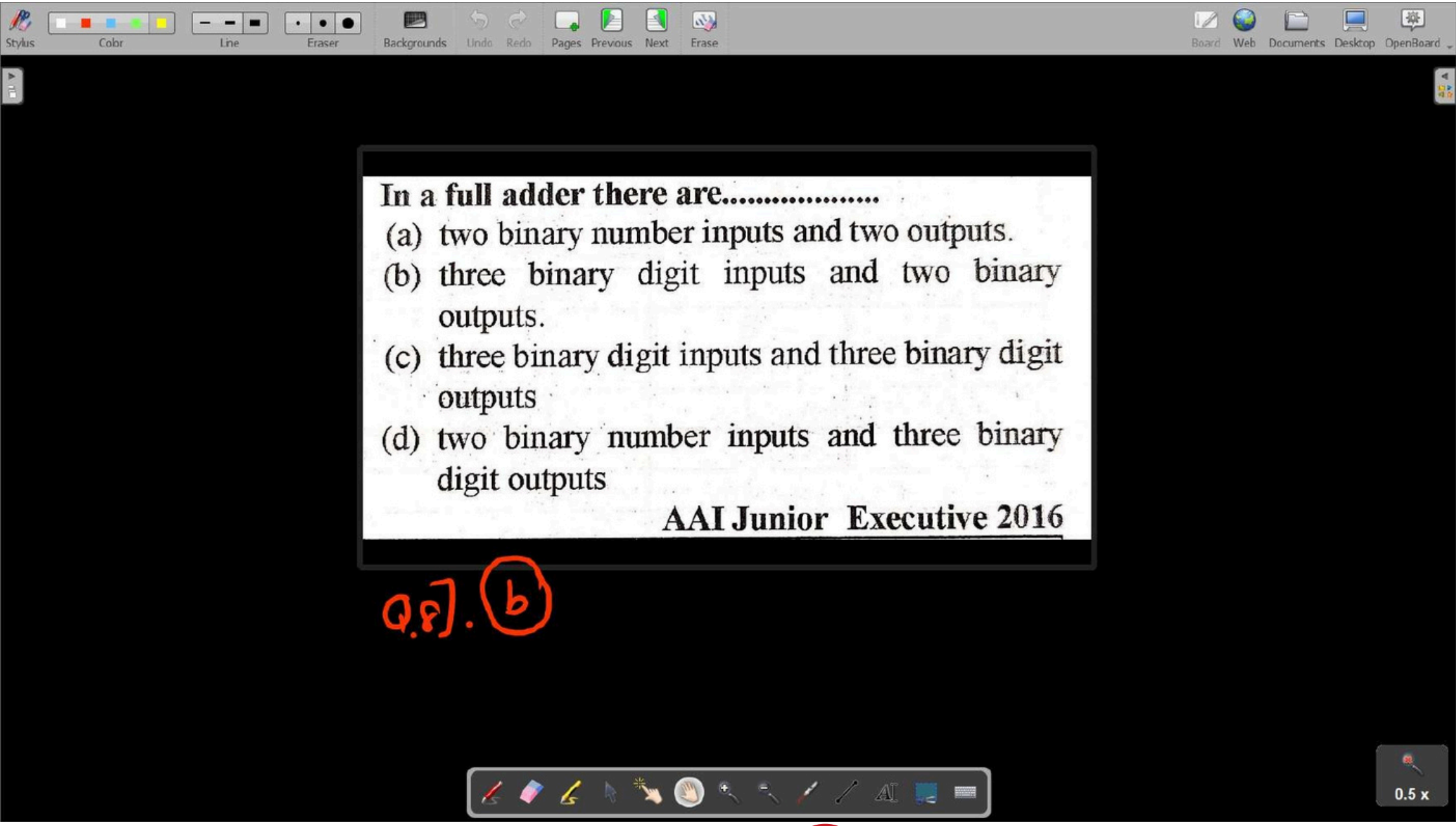
(A)

Q.7]. $f = \bar{S}_1\bar{S}_0 3 + \bar{S}_1 S_0 2 + S_1\bar{S}_0 1 + S_1 S_0 0$

$= \bar{S}_1\bar{S}_0 + S_1 S_0.$

$= \bar{x}\bar{y} + xy$ = Ex-NOR.

Full Video Link



Full Video Link

A full adder circuit has–

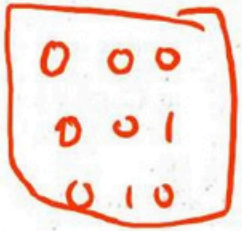
(a) two inputs and one output

(b) two inputs and two outputs

(c) three inputs and one output

(d) three inputs and two outputs

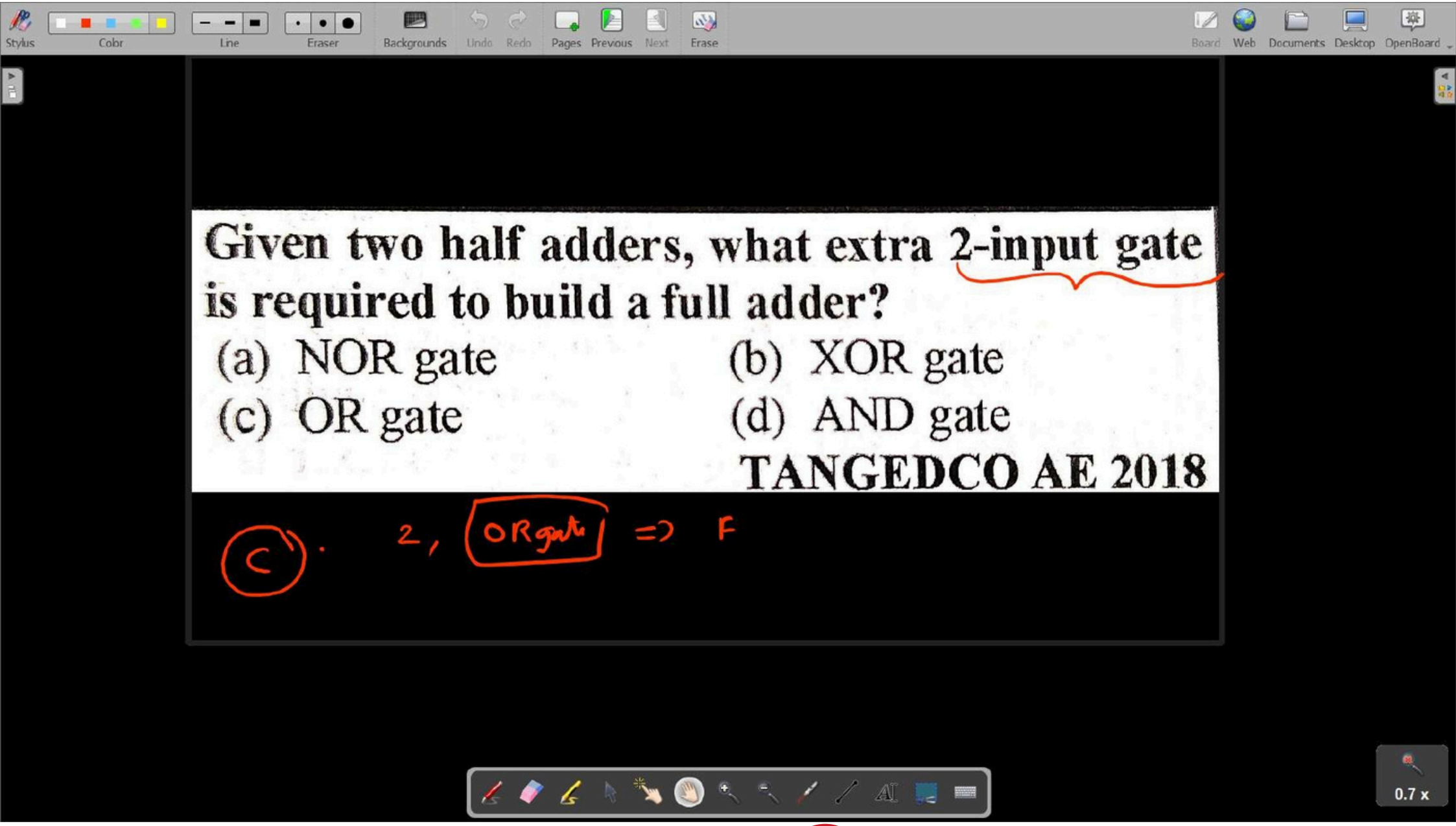
UKPSC AE 2012 Paper-I



A B
C_{in} ⇒ S, C.

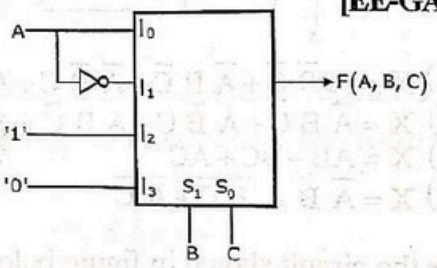
Q.9] . (b) . 2 → I/P → ⇒ S, C.

Full Video Link



A 4x1 MUX is used to implement a 3-input Boolean function as shown in figure. The Boolean function F(A,B,C) implemented is

[EE-GATE'06]



(A) $F(A,B,C)=\Sigma(1,2,4,6)$
(B) $F(A,B,C)=\Sigma(1,2,6)$
(C) $F(A,B,C)=\Sigma(2,4,5,6)$
(D) $F(A,B,C)=\Sigma(1,5,6)$

Q.1]. $F = \bar{S}_1\bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1\bar{S}_0 I_2 + S_1 S_0 I_3$.

$= \bar{B}\bar{C}A + \bar{B}C\bar{A} + B\bar{C}$

$= A\bar{B}\bar{C} + \bar{A}\bar{B}C + B\bar{C}[A+\bar{A}]$.

$F(A,B,C) = A\bar{B}\bar{C} + \bar{A}\bar{B}C + AB\bar{C} + \bar{A}B\bar{C}$.

$= \underset{4}{100} + \underset{1}{001} + \underset{6}{110} + \underset{2}{010}$.

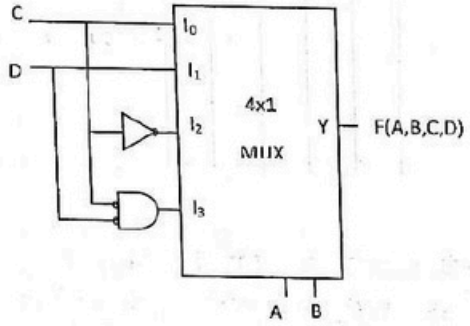
$= \Sigma_m(1,2,4,6)$

(A).

0.5 x

Full Video Link

The Boolean function realized by the logic circuit shown is **[EC-GATE '10]**



(A) $F=\sum m(0,1,3,5,9,10,14)$
(B) $F=\sum m(2,3,5,7,8,12,13)$
(C) $F=\sum m(1,2,4,5,11,14,15)$
(D) $F=\sum m(2,3,5,7,8,9,12)$

Q.2]. $Y = \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3$

$I_0 = C \quad I_1 = D \quad I_2 = \bar{C}$

$I_3 = \bar{C}.\bar{D}$.

$Y = \bar{A}\bar{B}C + \bar{A}BD + A\bar{B}\bar{C} + AB\bar{C}\bar{D}$.

$= \bar{A}\bar{B}C[D+\bar{D}] + \bar{A}BD[C+\bar{C}] + A\bar{B}\bar{C}[D+\bar{D}] + AB\bar{C}\bar{D}$.

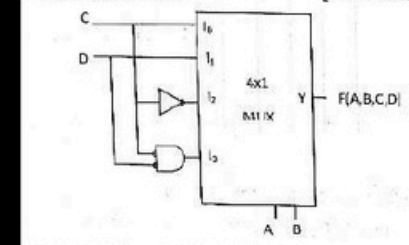
$= \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BCD + \bar{A}B\bar{C}D + A\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D}$.

$= 0011 + 0010 + 0111 + 0101 + 1001 + 1000 + 1100$

$= \sum m(2,3,5,7,8,9,12)$

(D).

The Boolean function realized by the logic circuit shown is [EC-GATE '10]



(A) $F=\sum m(0,1,3,5,9,10,14)$
(B) $F=\sum m(2,3,5,7,8,12,13)$
(C) $F=\sum m(1,2,4,5,11,14,15)$
(D) $F=\sum m(2,3,5,7,8,9,12)$

(D).

Q.2]. $Y = \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3$

$I_0 = C \quad I_1 = D \quad I_2 = \bar{C}$

$I_3 = \bar{C}.\bar{D}$.

$Y = \bar{A}\bar{B}C + \bar{A}BD + A\bar{B}\bar{C} + AB\bar{C}\bar{D}$.

$= \bar{A}\bar{B}C[D+\bar{D}] + \bar{A}BD[C+\bar{C}] + A\bar{B}\bar{C}[D+\bar{D}]$
$+ AB\bar{C}\bar{D}$.

$= \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BCD + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D +$
$A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D}$.

$= 0011 + 0010 + 0111 + 0101 + 1001 +$
$1000 + 1100$

$= \Sigma m(3,2,7,5,9,8,12)$

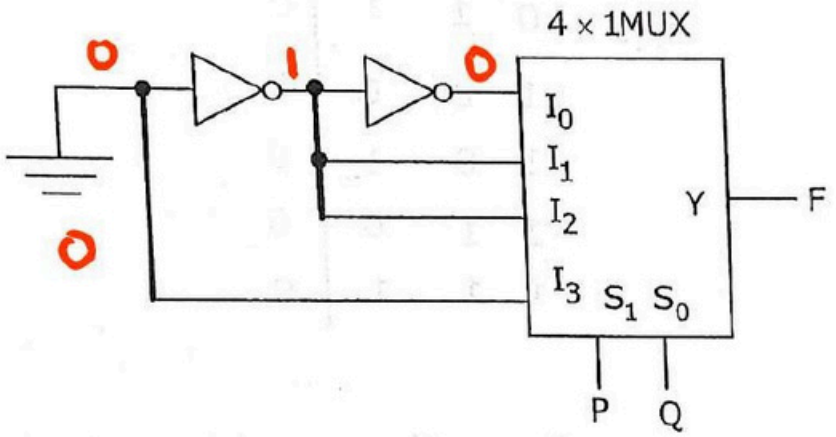
$= \Sigma m(2,3,5,7,8,9,12)$.

0.4 x

Full Video Link

The logic function implemented by the circuit below is (ground implies logic 0)

[EC-GATE'11]



(A) F = AND(P,Q)

(B) F = OR(P,Q)

(C) F = XNOR(P,Q)

(D) F = XOR(P, Q)

Q.3].

$F = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$.

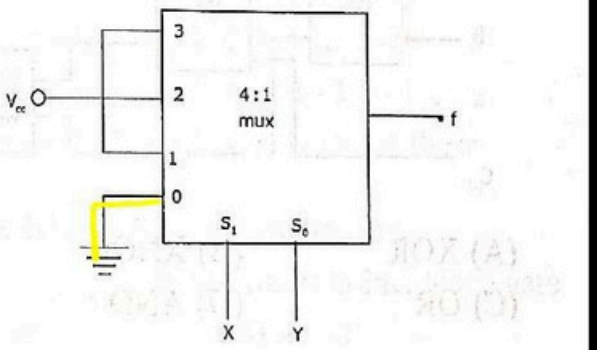
$I_0 = 0$ $I_1 = 1$ $I_2 = 1$ $I_3 = 0$.

(d).

$= \bar{P} Q + P \bar{Q}$.

Full Video Link

The output of the 4:1 mux shown in below figure is



(A) $\overline{(xy)} + x$ (B) $x+y$

(C) $\bar{x} + \bar{y}$ (D) $xy+\bar{x}$

Q.4].

$f = \bar{S}_1 \bar{S}_0 0 + \bar{S}_1 S_0 1 + S_1 \bar{S}_0 2 + S_1 S_0 3$

$= \bar{x}y + x\bar{y} + xy.$

$= \bar{x}y + xy + x\bar{y}.$

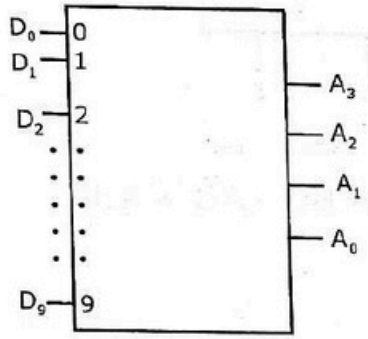
$= y[\bar{x} + x] + x\bar{y}.$

$= y + x\bar{y} = (y+x)(y+\bar{y})$

(B).

Full Video Link

Consider the following Circuit and answer the question below. Assume A_3 MSB, D_9 MSB



For a decimal to BCD encoder for D_6 to be high, what will be the output?

(A) $A_0 = 1, A_1 = 0, A_2 = 0, A_3 = 0$

(B) $A_0 = 0, A_1 = 1, A_2 = 1, A_3 = 1$

(C) $A_0 = 0, A_1 = 1, A_2 = 1, A_3 = 0$

(D) $A_0 = 1, A_1 = 1, A_2 = 1, A_3 = 1$

D0 →

D1 →

D6 →

A0 = 0

A1 = 1

A2 = 1

A3 = 0.

0 0 0 0

0 0 0 1

0 1 1 0 .

A3 A2 A1 A0.

0

1

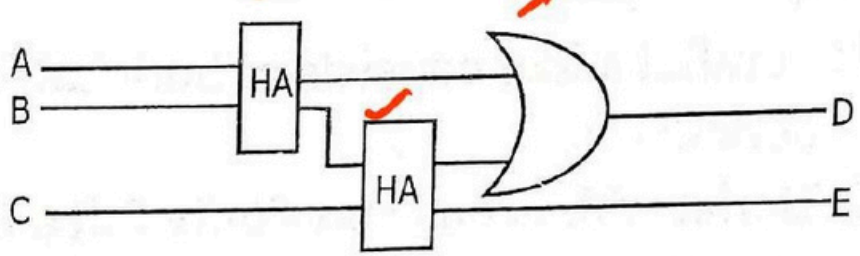
1

0 .

0.7 x

Full Video Link

The given figure is of a



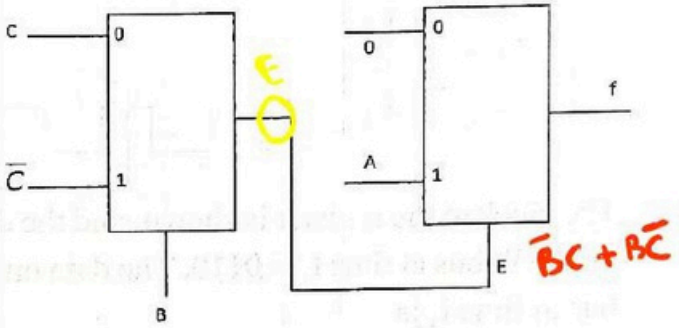
(A) Full adder (B) Full subtractor

(C) Parity checker (D) None of these

A

Full Video Link

The Boolean function f implemented in figure using two input multiplexers is [EC-GATE '05]



(A) $A\bar{B}C + AB\bar{C}$

(B) $ABC + A\bar{B}\,\bar{C}$

(C) $\bar{A}BC + \bar{A}\,\bar{B}\,\bar{C}$

(D) $\bar{A}\,\bar{B}C + \bar{A}B\bar{C}$

Q.7].

$E = \bar{B}0 + B1$

$= \bar{B}C + B\bar{C}$.

(A).

$f = \bar{E}0 + E1$

$= EA$

$= (\bar{B}C + B\bar{C})A = A\bar{B}C + AB\bar{C}$.

0.5 x

Full Video Link

Sequential Circuit.

Flip Flops.

* NOR gate ⇒ anyone of I/p is 1 then output = 0.

* NAND gate ⇒ anyone of its I/p is 0 then output = 1.

SR Flip Flop : $Q_{n+1} = S + \bar{R} Q_n$

Jk Flip Flop : $Q_{n+1} = J\bar{Q}_n + \bar{k} Q_n$

D Flip Flop : $Q_{n+1} = D$

T Flip Flop : $Q_{n+1} = T\bar{Q}_n + \bar{T} Q_n$.

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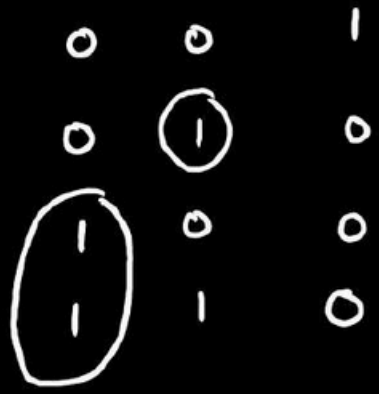
T.T → NOR.



T.T → NAND.

Sequential Circuit.

Flip Flops.

* NOR gate ⇒ anyone of I/p is 1 then output = 0.

* NAND gate ⇒ anyone of its I/p is 0 then output = 1.

SR Flip Flop : $Q_{n+1} = S + \bar{R} Q_n$

Jk Flip Flop : $Q_{n+1} = J\bar{Q}_n + \bar{K} Q_n$

D Flip Flop : $Q_{n+1} = D$

T Flip Flop : $Q_{n+1} = T\bar{Q}_n + \bar{T} Q_n$.

2.0 x

Full Video Link

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If J = K in case of J – K flip-flop, then the resulting flip-flop is known as:

(a) J-K FLIP FLOP itself
(b) T-type FLIP-FLOP
(c) S-R FLIP-FLOP
(d) D-type FLIP-FLOP

Q.1].

b

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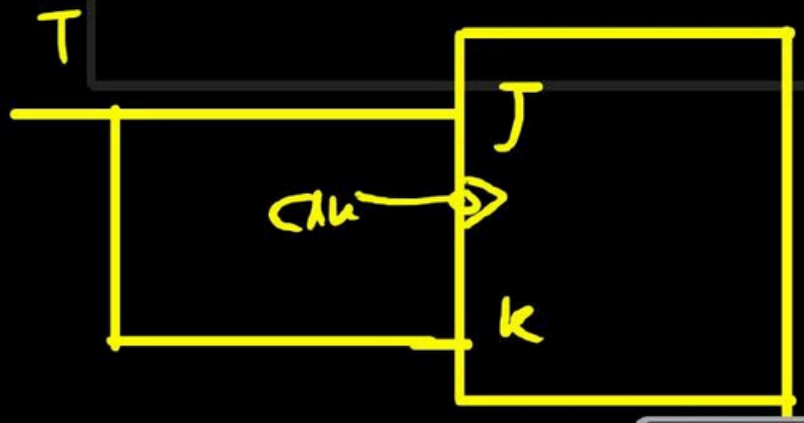
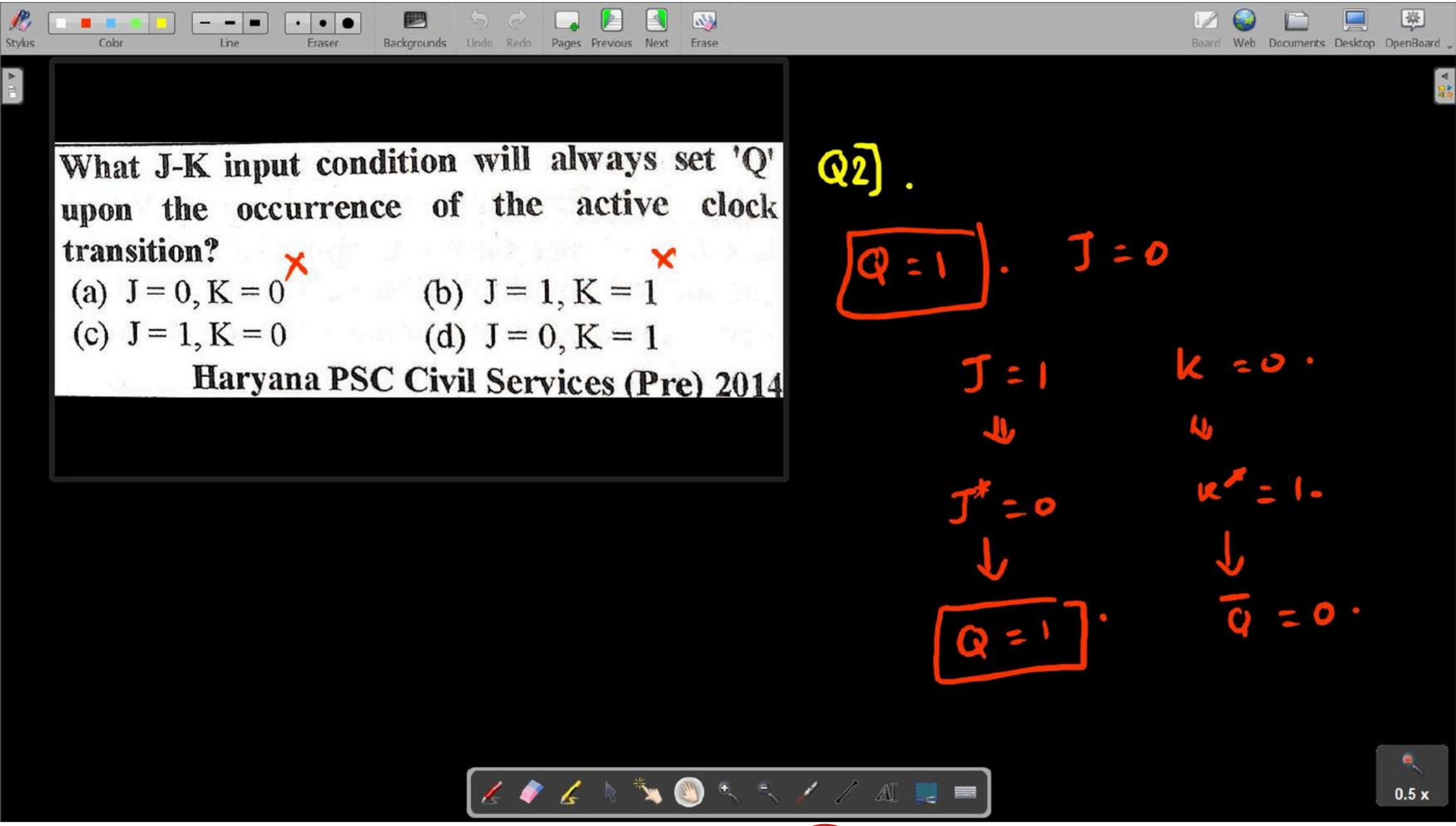


0.7 x

Full Video Link



Full Video Link

In a J-K flip-flop, if $J = \overline{K}$, then it acts as a/an:

(a) T flip-flop
(b) D flip-flop
(c) RS flip-flop
(d) Decoder

LMRC AM 2020

Q.3]. $J = K \Rightarrow$ TFF.

$J = \overline{K} \Rightarrow$ DFF

(b)

Full Video Link

In a master slave JK-flip-flop J = K = 1. The state Q_{n+1} of the flip-flop after the clock pulse will be :

(a) 0

(b) 1

(c) Q_n

(d) $\bar{Q}_n$

MPSC (Mains) 2018 Paper-I

Q.4]. $\bar{Q}_n$

J=K=1 => Toggle.

(D).

Full Video Link

The characteristic equation of the T - FF is given by

(a) $Q^+ = \bar{T}Q + T\bar{Q}$

(b) $Q^+ = T\bar{Q} + Q\bar{T}$

(c) $Q^+ = QT$

(d) $Q^+ = T\bar{Q}$

Q.5]

$Q_{n+1} = T \oplus Q_n$

$= T\bar{Q} + \bar{T}Q$

(b)

In a RS flip-flop, if S = 1 and R = 0, then the value of Q will be

(a) same
(b) 0
(c) 1
(d) undefined

$S = 0 \Rightarrow S^* = 1 \Rightarrow Q = 0$

$R = 1 \Rightarrow R^* = 0 \Rightarrow \bar{Q} = 1$

UKPSC AE 2007, Paper-I

Q.6. $S = 1 \Rightarrow S^* = 0 \Rightarrow Q = 1$

$R = 0 \Rightarrow R^* = 1 \Rightarrow \bar{Q} = 0$

(c)

Full Video Link

The following flip-flop is used to eliminate race-around problem:

(a) R-S flip-flop
(b) Master Slave flip-flop
(c) J-K flip-flop
(d) None of these

UKPSC AE 2007 Paper-II

Q.8]. Master Slave FlipFlop.

Full Video Link

A D-flip flop function is obtained from J–K flip flop. If the flip flop belongs to a TTL family the connection needed at the input must be

(a) J = 1 and K = 1

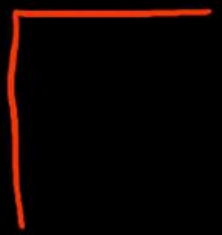
(b) J = 1 and K = 0

(c) J = K = 0

(d) J = 0 and K = 1

UPPCL AE 2015

Q.9].



i]. (a) only correct

ii]. (b) only correct

iii]. (d) only correct.

iv]. (b) and (d) correct.

Full Video Link

Which one of the following is not a sequential circuit / system ?

(a) Clocked S-R flip-flop (b) Shift register

(c) ROM (d) Ripple counter

UKPSC AE 2012 Paper-II

i]. (a), (b) and (d) only correct.

ii]. (b) and (c) only correct

iii]. (a) only correct

iv]. (c) only correct.

Full Video Link

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Master-slave J-K flip-flop is used to

(a) Eliminate race around condition

(b) Improve its reliability

(c) Reduce power dissipation

(d) Increase its clock frequency

Rajasthan Nagar Nigam AE 2016, Shift-I

(A)

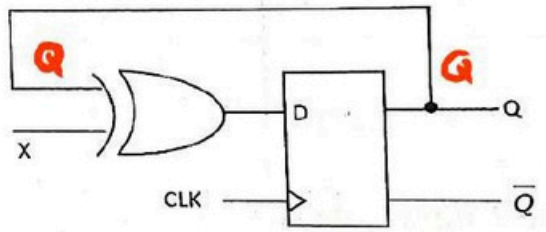
6383369767

0.7 x

Full Video Link

The digital circuit shown in figure works as a

[EE-GATE '05]



(A) JK flip-flop
(B) Clocked RS flip-flop
(C) T flip-flop
(D) Ring counter

(C)

Q.1]. $D = x\bar{Q} + Q\bar{x}$

$= x \oplus Q.$

$\downarrow$

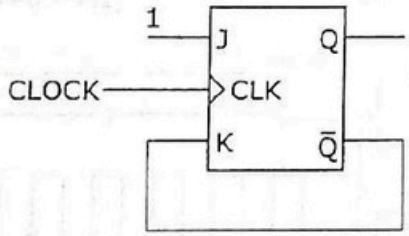
T

$D = T \oplus Q$

Full Video Link

In the figure shown, the initial state of Q is 0. The output is observed after the application of each clock pulse. The output sequence at Q is

[IN-GATE '09]



(A) 0000…
(B) 1010…
(C) 1111…
(D) 1000…

Q.2] . Q = 0.

Clk	J	K = $\bar{Q}$	Q	$\bar{Q}$
Initial 0	x	x	0	1
1st	1	1	1	0
2nd	1	0	1	0
3rd	1	0	1	0
4th	1	0	1	0
5th	1	0	1	0

(C) . J . K

J: 1 ↓ 0 ↓

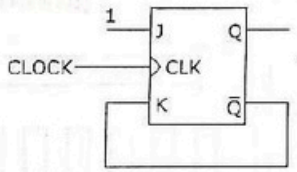
K: 0 ↓ 1 ↓

1 1 1 1 1 . . . .

Full Video Link

In the figure shown, the initial state of Q is 0. The output is observed after the application of each clock pulse. The output sequence at Q is

[IN-GATE '09]



(A) 0000… (B) 1010…

(C) 1111… (D) 1000…

Q.2]. Q = 0.

Clk	J	$K = \bar{Q}$	Q	$\bar{Q}$
Initial	x	x	0	1
1st	1	1	1	0
2nd	1	0	1	0
3rd	1	0	1	0
4th	1	0	1	0
5th	1	0	1	0

(c) J: 1 ↓ 0 ↓ 1 ; K: 0 ↓ 1 ↓ 0 ; 1 1 1 1 1 ....

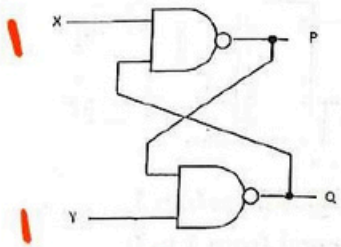
Full Video Link

The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below:

[EC-GATE '07]

X = 0, Y = 1; X = 0, Y = 0; X = 1, Y = 1.

The corresponding stable P, Q outputs will be:



(A) P=1, Q=0; P=1, Q=0; P=1, Q=0 or P=0, Q=1

(B) P=1, Q=0; P=0, Q=1; or P=0, Q=1; P=0, Q=1

(C) P=1, Q=0; P=1, Q=1; P=1, Q=0 or P=0, Q=1

(D) P=1, Q=0; P=1, Q=1; P=1, Q=1

Q.3]. X = 0 Y = 1 P = 1 Q = 0.

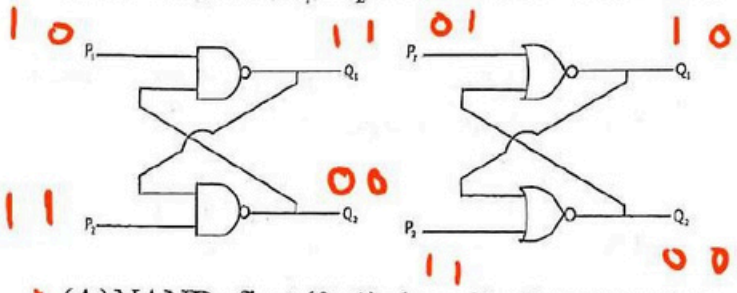
X = 0 Y = 0 ⇒ P = 1 Q = 1 ⇒ X

Q = 1 $\bar{Q}$ = 1 ?

X	Y	Q	$\bar{Q}$
0	0	x	x

Full Video Link

Refer to the NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both the latches are first made (0, 1) and then, after a few seconds, made (1, 1). The corresponding stable outputs (Q_1, Q_2) are [EC-GATE '09]



(A) NAND: first (0, 1) then (0, 1) NOR: first (1, 0) then (0, 0)

(B) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (1, 1)

(C) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (0, 0)

(D) NAND: first (1, 0) then (1, 1) NOR: first (0, 1) then (0, 1)

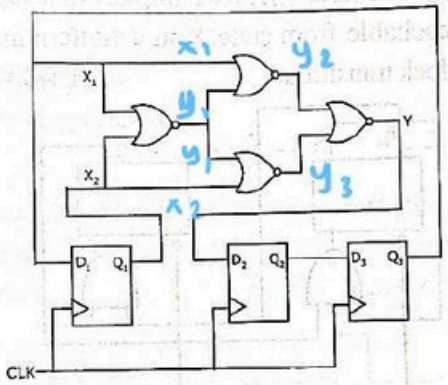
Q.4].

C

0.7 x

Full Video Link

The correct input-output relationship between Y and (X_1, X_2) is [IN-GATE '07]



(A) $Y = X_1 + X_2$ (B) $Y = X_1 X_2$

(C) $Y = X_1 \oplus X_2$ (D) $Y = \overline{X_1 \oplus X_2}$

Q.5. $y_1 = \overline{x_1 + x_2} = \bar{x}_1 \cdot \bar{x}_2$

$y_2 = x_1 + (\bar{x}_1 \cdot \bar{x}_2)$ $\quad \overline{A.B} = \bar{A} + \bar{B}$.

$= \bar{x}_1 \cdot (\overline{\bar{x}_1 \cdot \bar{x}_2})$

$= \bar{x}_1 \cdot (x_1 + x_2)$ 6383369767.

$= \bar{x}_1 \cdot x_1 + \bar{x}_1 x_2$

$y_2 = \bar{x}_1 x_2$ $\quad y = \overline{y_2 + y_3}$

$y = \overline{\bar{x}_1 x_2 + x_1 \bar{x}_2}$

$y_3 = \overline{y_1 + x_2}$

$= \overline{(\bar{x}_1 \cdot \bar{x}_2) + x_2}$ $= \overline{(\bar{x}_1 \cdot \bar{x}_2)} \cdot \bar{x}_2$

$= \overline{x_1 \oplus x_2}$ $= x_1 \odot x_2$.

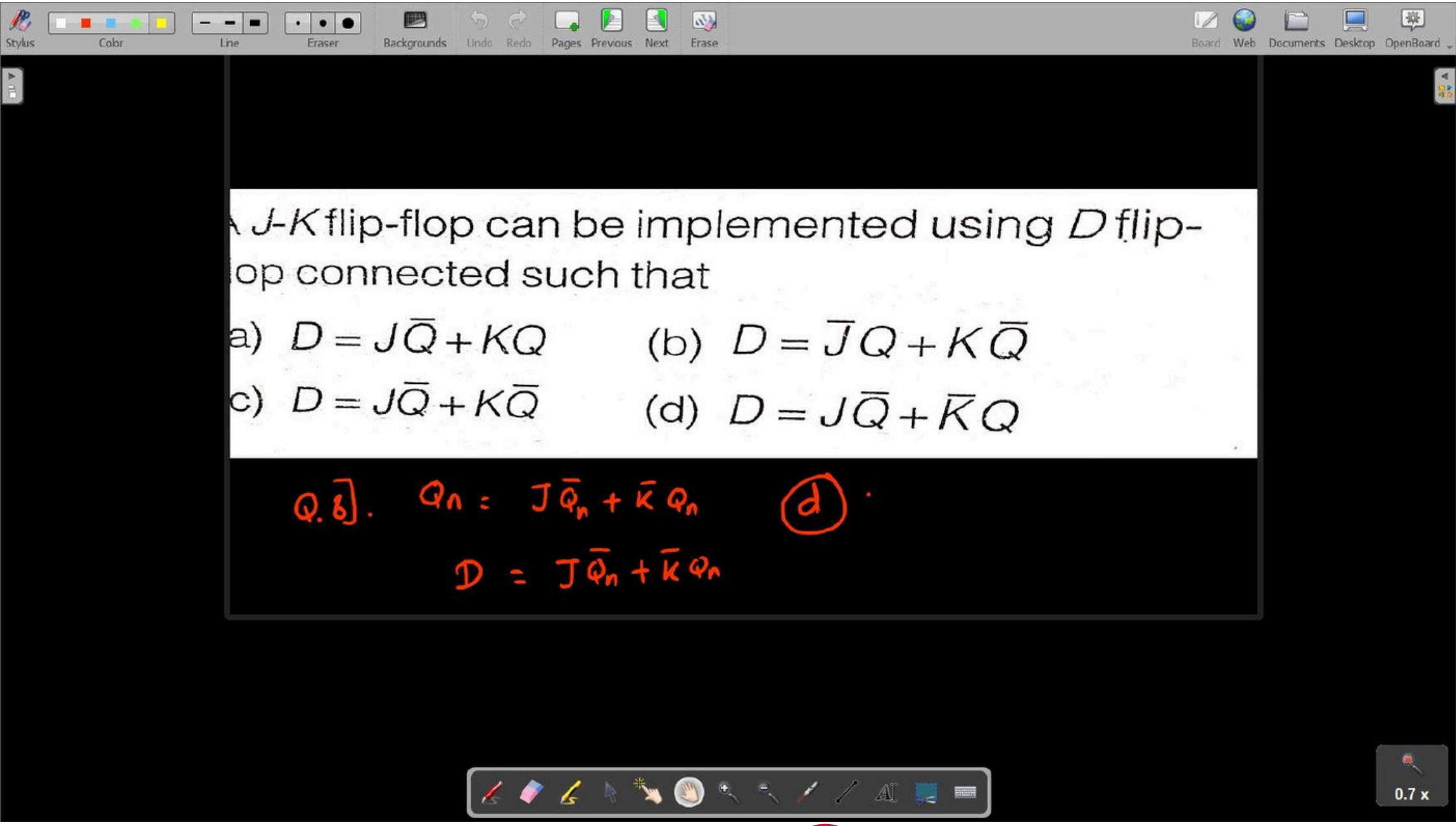
$= x_1 x_2 + \bar{x}_1 \bar{x}_2$.

$= (x_1 + \bar{x}_2) \cdot \bar{x}_2$

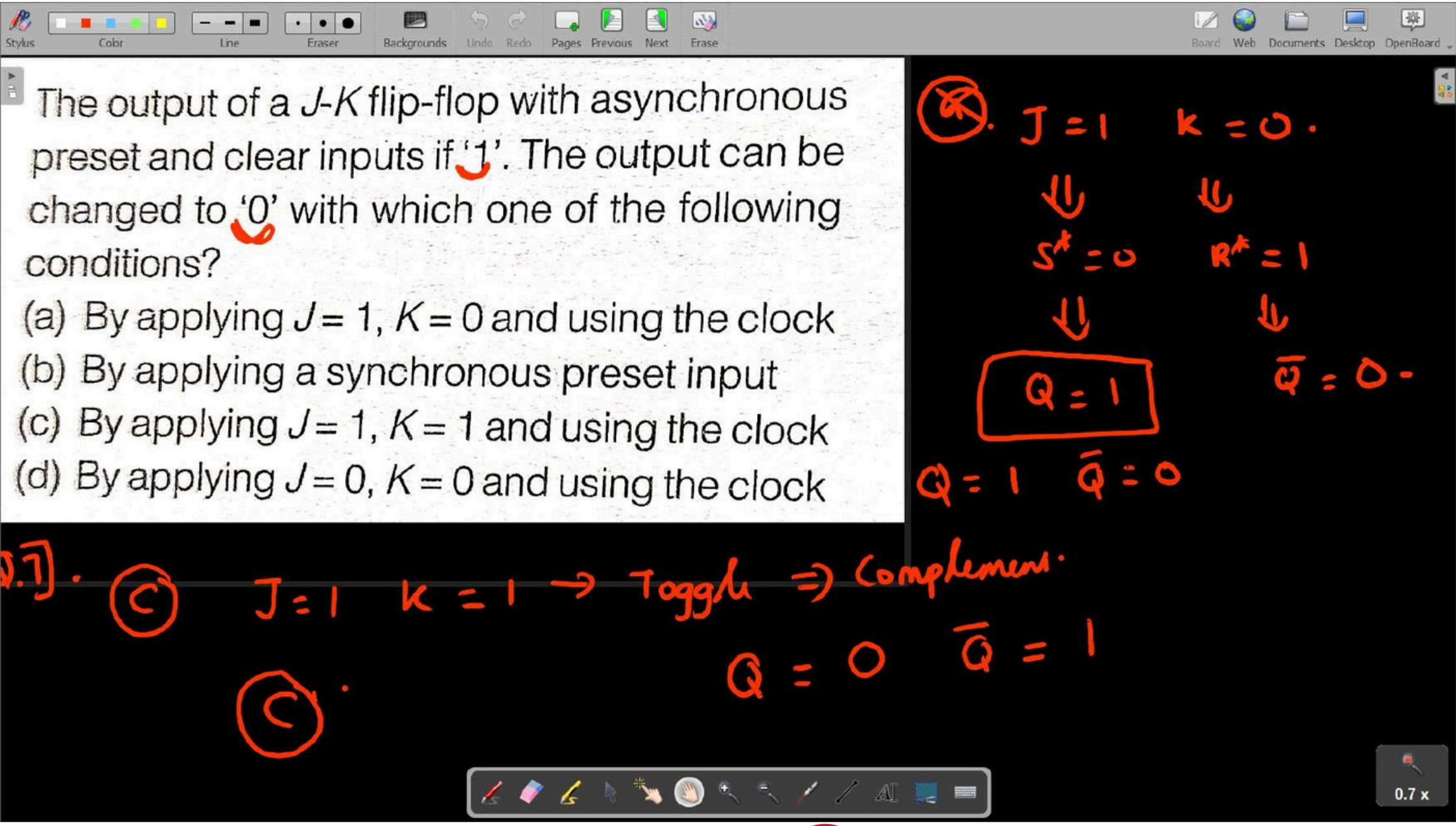
$= x_1 \bar{x}_2 + x_2 \bar{x}_2$ $= x_1 \bar{x}_2 = y_3$

(D).

Full Video Link



Full Video Link



Full Video Link

In a clocked *S-R* flip-flop made with NAND gates, the input combination $S = 1$, $R = 1$, is not permitted because it leads to

(a) a race around condition.

(b) both the outputs being zero simultaneously.

(c) an unpredictable output when the inputs become zero.

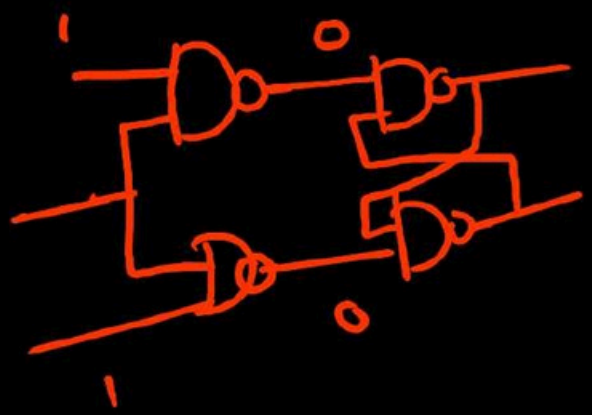
(d) the output becoming available before the clock goes low.

Q.8]. S=1 R=1

(c)

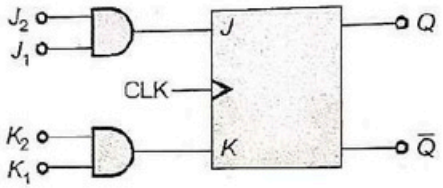
$S^* = 0$ $R^* = 0$

$Q = 1$ $\bar{Q} = 1$



Full Video Link

For the flip-flop shown below, there is one clock pulse for each bit time.



If the following serial data are applied to the flip-flop, then the resulting decimal value of the serial data that appears on the Q output will be (assume that, Q is initially '0')

$J_1 = 01101101$; $J_2 = 10011011$

$K_1 = 01101001$; $K_2 = 11011011$

(a) 14 (b) 24

(c) 18 (d) 20

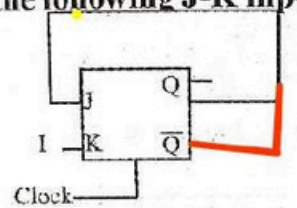
A

clk	$J = J_2 J_1$	$K = K_2 K_1$	Q	$\overline{Q}$
0	x	x	0	1
1	0	0	0	1
1	0	1	0	1
1	0	0	0	1
1	0	0	0	1
1	0	1	1	0
1	0	0	1	0
1	0	1	0	1

0 0 0 0 1 1 1 0

→ 1 0

Consider the following J-K flip-flop:



In the above J-K flip-flop, J = $\overline{Q}$ and K=1. Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

(a) 010000 (b) 011001
(c) 010010 (d) 010101

RPSC AE 2018

Q.10]. K=1 $J = \overline{Q}$ Q=0 $\overline{Q}$ = 1

Clk	J	K	Q	$\overline{Q}$
0	x	x	0	1
1st	1	1	1	0
2nd	0	1	0	1
3rd	1	1	1	0
4th	0	1	0	1
5th	1	1	1	0
6th	0	1	0	1

Set ⇒ Q = 1 $\overline{Q}$ = 0.

Reset ⇒ Q = 0 $\overline{Q}$ = 1.

0 1 0 1 0 1 0.

(b)

Full Video Link

. Counters and Registers.

Counters:

Types: * Asynchronous Counter * Synchronous counter.

3bit

→ up counter (0, 1, 2, ...)

→ down counter (7, 6, ...)

→ up / down counter.

1. Asynchronous:

n-bit count ⇒ n FlipFlops Required.

⇒ Maximum count = $2^n - 1$.

⇒ 2 bit Counter ⇒

Mod 4 counter
Mod 8 counter
} Cascaded.

Full Video Link

. Counters and Register.

Counters:

Types: * Asynchronous Counter * Synchronous counter.

3 bit

→ up counter (0, 1, 2, ...)

→ down counter (7, 6, ...)

→ up/down counter.

1. Asynchronous:

n-bit Count ⇒ n Flip Flops Required.

⇒ Maximum Count = $2^n - 1$.

⇒ 2 bit Counter ⇒ 2^2 = Mod 4.

⇒ 3 bit Counter ⇒ 2^3 = Mod 8.

⇒ n bit Counter ⇒ Mod 2^n.

Mod 4 Counter, Mod 8 Counter } Cascaded.

New Mod = Mod 4 × Mod 8.

2. Synchronous Counter: [Simultaneous Clk pulse].

2 bit up Counter:

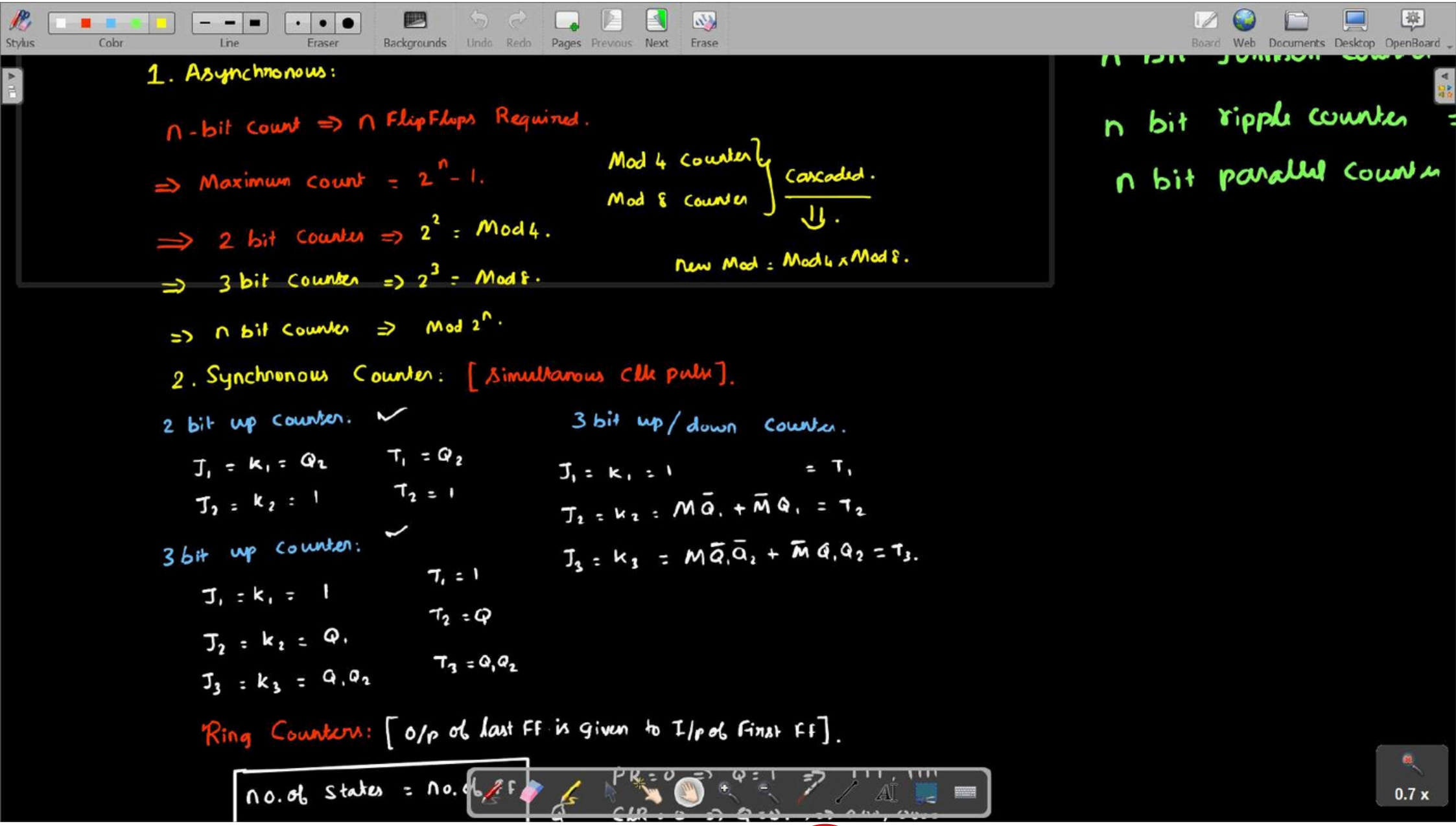
3 bit up/down Counter.

$T_1 = K_1 = Q_2$

* Serial Inp
* Serial Inpu
* Parallel Inp
* Parallel Inpu
n bit ring co
n bit Johnson
n bit ripple c
n bit parallel

0.7 x

Full Video Link



Full Video Link

2 bit up counter:

$J_1 = K_1 = Q_2$ $\quad T_1 = Q_2$

$J_2 = K_2 = 1$ $\quad T_2 = 1$

3 bit up counter:

$J_1 = K_1 = 1$ $\quad T_1 = 1$

$J_2 = K_2 = Q_1$ $\quad T_2 = Q$

$J_3 = K_3 = Q_1 Q_2$ $\quad T_3 = Q_1 Q_2$

3 bit up / down counter.

$J_1 = K_1 = 1 \quad = T_1$

$J_2 = K_2 = M\bar{Q}_1 + \bar{M}Q_1 = T_2$

$J_3 = K_3 = M\bar{Q}_1\bar{Q}_2 + \bar{M}Q_1Q_2 = T_3$.

Ring Counters: [O/p of last FF is given to I/p of First FF].

no. of States = no. of FF

PR = 0 $\Rightarrow$ Q = 1 $\Rightarrow$ 111, 1111

CLR = 0 $\Rightarrow$ Q = 0. $\Rightarrow$ 000, 0000

Johnshon's FF (Twisted / switch tail).

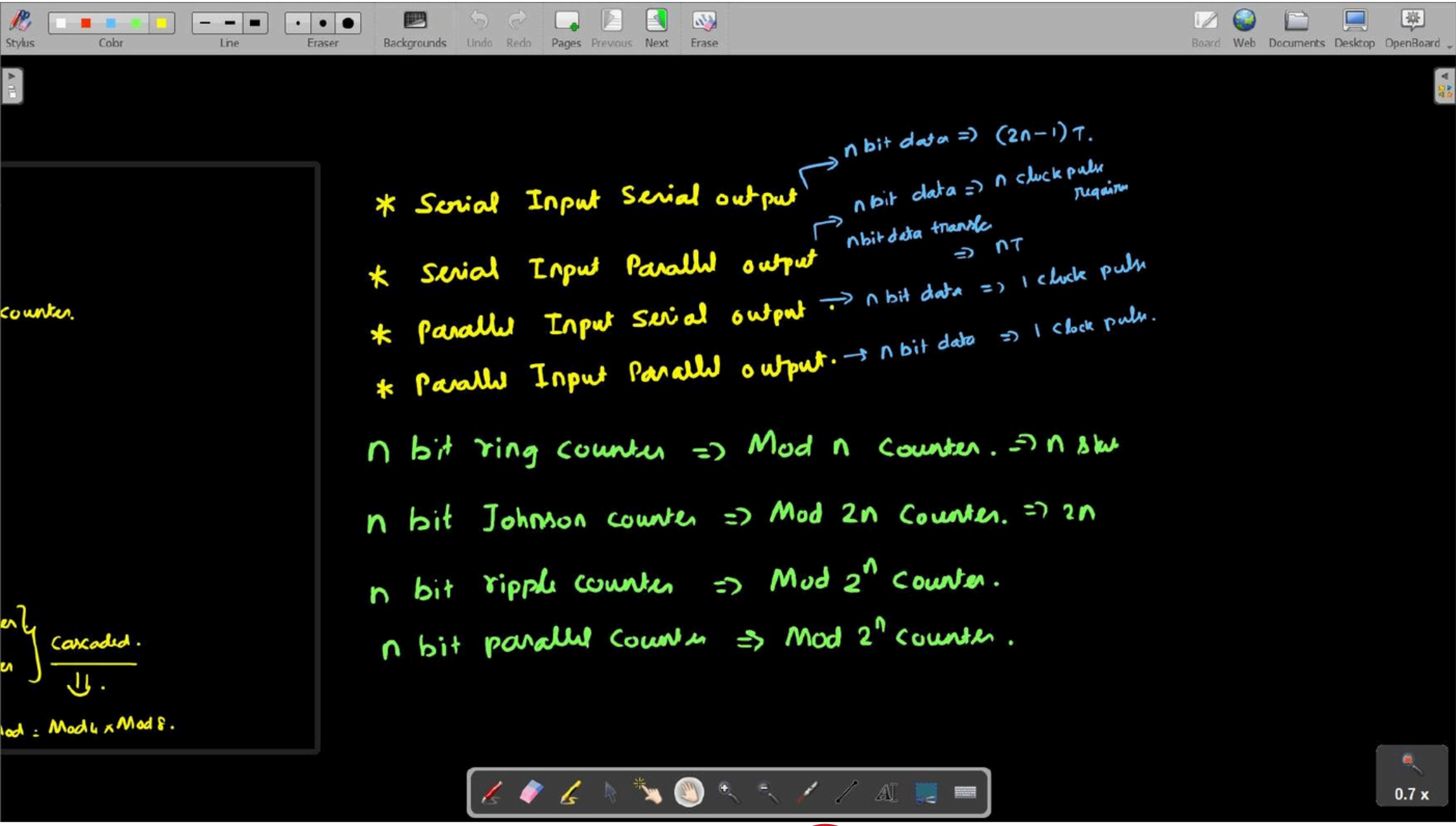
no. of states = 2 × no. of FF

$$\frac{1}{T_c} = f_c \leq \frac{1}{n\, t_{pd}}.$$

Clock Frequency = f_c

Propagation delay = t_{pd}.

n = no. of States



Full Video Link

A pulse train with a frequency 1 MHz is counted using a Mod 1024 ripple counter build with J-K flip-flop. Maximum permissible propagation delay per flip-flop is

(A) 10 n sec (B) 100 n sec

(C) 1000 n sec (D) 10^4 n sec

$t_{pd} = ?$

$f_c \leq \frac{1}{n t_{pd}} \Rightarrow t_{pd} \leq \frac{1}{f_c . n}$

n = no. of states

Q.1]. $f_c = 1\,MHz = 1 \times 10^6\,Hz$. n = no. of states.

MOD 1024 = Mod 2^n = 10 States = 10 bit ripple counter.

$t_{pd} = \frac{1}{10 \times 1 \times 10^6} = 10^{-7}$ secs. 10^{-7}.

$= 100 \times 10^{-9}$ sec = 100 n secs.

(B)

If a Mod 14 and Mod 20 counter are cascaded, what will be the new Mod number?

(A) 34 (B) 280 (C) 6

(D) Will not be a counter any more

Cascaded ⇒ Mod 14 x Mod 20 = 280 Mod

= Mod 280.

Full Video Link

What is the frequency of output of last flip-flop for an input clock frequency of 5 MHz in a Mod-1024 counter?

(A) 4.833 kHz (B) 4833 kHz

(C) 48330 Hz (D) 4833 MHz

$f_c = 5\,MHz.$

$n = 10.$

$f_{MSB} = f_{last} = \frac{f_c}{2^n}.$

$= \frac{5 \times 10^6}{1024}$

$= 4882.8 = 4883$ Hz.

(B)

Full Video Link

How many flip-flops are required to build a binary counter to count from 0 to 1023? What is the MOD number?

(A) 1024, 1024 (B) 10, 1023

(C) 10, 1024 (D) 10, 10

1023 => ?

↳ 1023

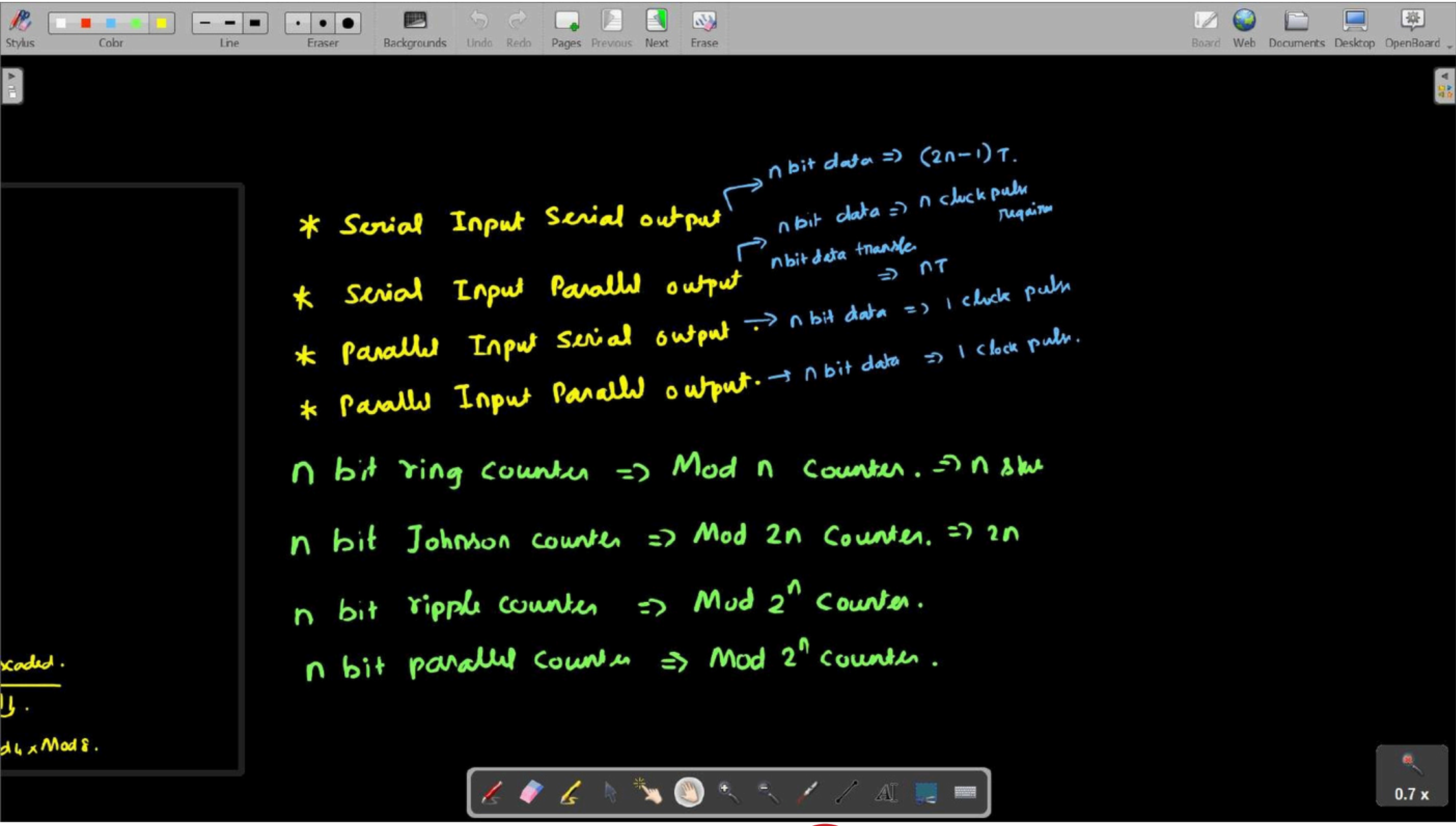
1024 => 2^n

n = 10.

10 FF required = 10 state => Mod 2^{10} => Mod 1024.

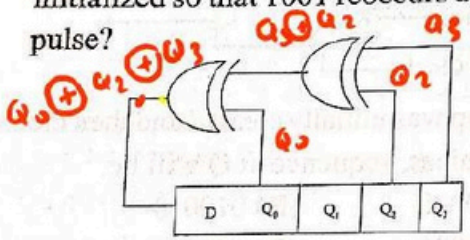
(C).

Full Video Link



Full Video Link

To what value should the shift register be initialized so that 1001 reoccurs after 1st clock pulse?



(A) 0000
(B) 0010
(C) 0100
(D) 0011

Q.1]. $Q_0 \oplus Q_2 \oplus Q_3$ $0 \oplus 0 \oplus 0$

Clk	I/p D	Q_0	Q_1	Q_2	Q_3
Initial	x	0	0	0	0
I	0	0	0	0	0
Initial	x	0	0	1	0
I	1	1	0	0	1

I/p => $Q_0 \oplus Q_2 \oplus Q_3$

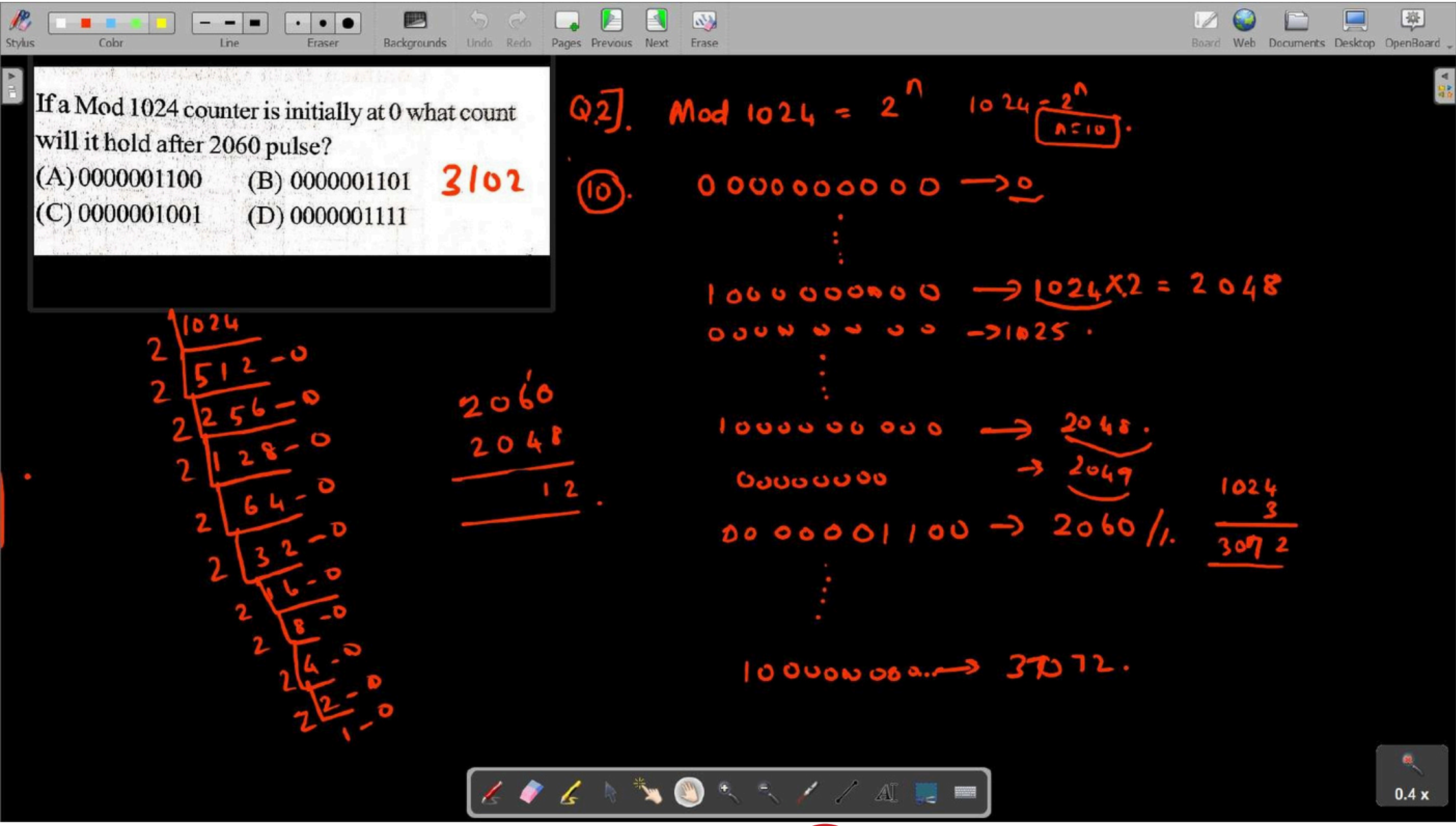
(A) (B)

0 0 0 0

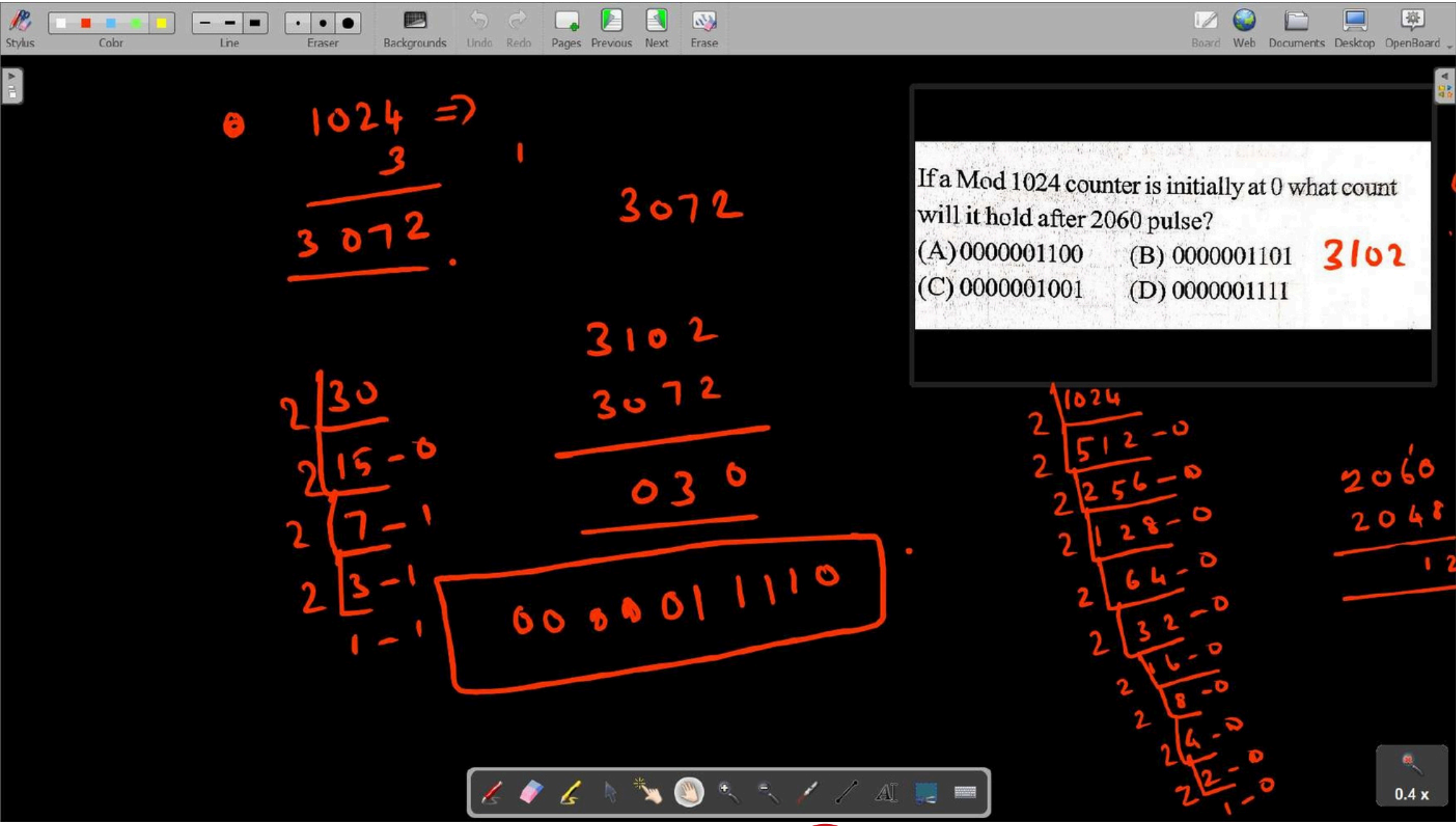
0 0 1 0

0 ⊕ 1 ⊕ 0

Full Video Link

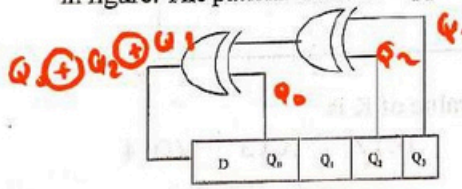


Full Video Link



Full Video Link

A 4 bit shift register is initialized to value 1000 for (Q_3, Q_2, Q_1, Q_0). The D input is derived from Q_0, Q_2 and Q_3 through two XOR gates as shown in figure. The pattern 1000 will appear at



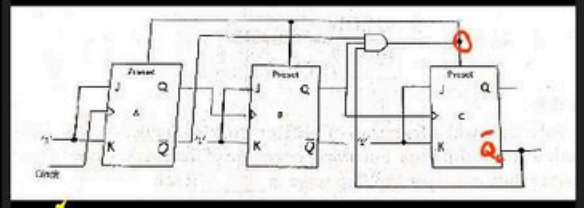
(A) 3rd pulse (B) 7th pulse

(C) 6th pulse (D) 4th pulse

Q.3

clk	I/p D	Q_0	Q_1	Q_2	Q_3
Initial	x	1	0	0	0
I	1	1	0	0	0
II	1	1	1	0	0
III	0	0	1	1	0
IV	0	0	0	1	1
V	0	0	0	0	1
VI	1	1	0	0	0

The ripple counter shown in figure as



A]. Mod 3 up counter ✗ B]. Mod 3 down counter.

C]. Mod 5 up counter ✗ D]. Mod 5 down counter.

EC → GATE 1999.

$0 \times 1 \times 0 = 0$

Q.4] $P = \bar{Q}_A Q_B \bar{Q}_C = 1 \Rightarrow$

Clk	Q_A	Q_B	Q_C	P
Initial	1	1	1	0
I	1	1	0	0
II	1	0	1	0
III	1	0	0	0
IV	0	1	1	0
V	0	1	0	1
VI	0	0	1	
VII	0	0	0	

$\bar{Q}_A Q_B \bar{Q}_C$

→ $P = 0.1.1 = 0$

→ $P = 0.0.0 = 0$

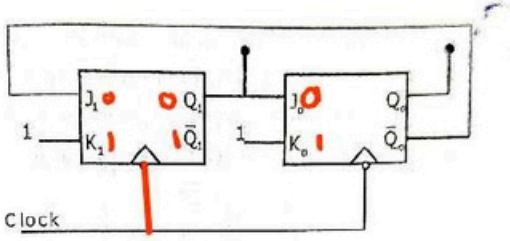
→ $P = 0 \times 0 \times 1 = 0$

→ $P = 1 \times 1 \times 0 = 0$

→ $P = 1 \times 1 \times 1 = 1$

Full Video Link

Consider the following MOD K counter:



The value of K is

(A) 1 (B) 2 (C) 3 (D) 4

Q.5]

$J_1 = 1 \quad K_1 = 1$

$\bar{Q}_0$		Q_1			
J_1	K_1	J_0	K_0	Q_1	Q_0
1	1	0	1	0	0
1	1	1	1	1	0
0	1	0	1	0	1
1	1	0	1	0	0
1	1	1	1	1	0

Mod 3

0.4 x

Full Video Link

If four bit data of 1011 is to be serially transmitted and serially to be received then the conversion time is (clock frequency is 1 MHz).

(A) 11μs (B) 8μs (C) 7μs (D) 3μs

$n = 4$

SISO $\Rightarrow (2N-1)T$ $\quad f_c = 1\,MHz$.

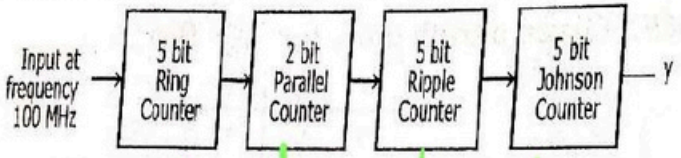
$\Rightarrow (2(4)-1) \times \left(\frac{1}{10^6}\right)$ $\quad T = \frac{1}{1\,MHz}$.

(C)

$= 7 \times 10^{-6}$ sec.

$= 7\,\mu$ secs.

The frequency of the pulse at output y in the combination of counter shown below



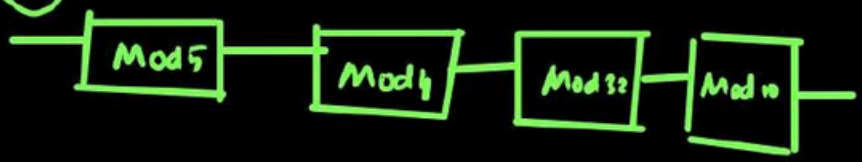
(A) 1MHz (B) 100kHz
(C) 0.5MHz (D) 15.625kHz.

$f_{out} = \frac{f_{in}}{\text{Mod number.}} = \frac{100 \times 10^6}{6400}$

$= \frac{500}{1000} \frac{250}{64} \frac{125}{32} \frac{16}{}$

$= 15,625\text{Hz}$.

(D) $= 15.625\text{KHz}$.



5 bit Ring Counter => Mod 5

2 bit parallel Counter => Mod 2^2 => Mod 4

5 bit Ripple Counter => Mod 2^5 => Mod 32.

5 bit Johnson Counter => Mod 2×5 => Mod 10.

32
2
6400

0.4 x

Full Video Link